

大同大學 101 學年度研究所碩士班入學考試試題

考試科目：電子學

所別：電機工程研究所

第 1/2 頁

註：本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

1. (16%) Find $V_1 \sim V_4$ and $I_1 \sim I_4$ in the circuit shown in Fig. 1. Assume $|V_{BE}|=0.7V$, $|V_{CE(sat)}|=0.2V$ and $\beta=\infty$.

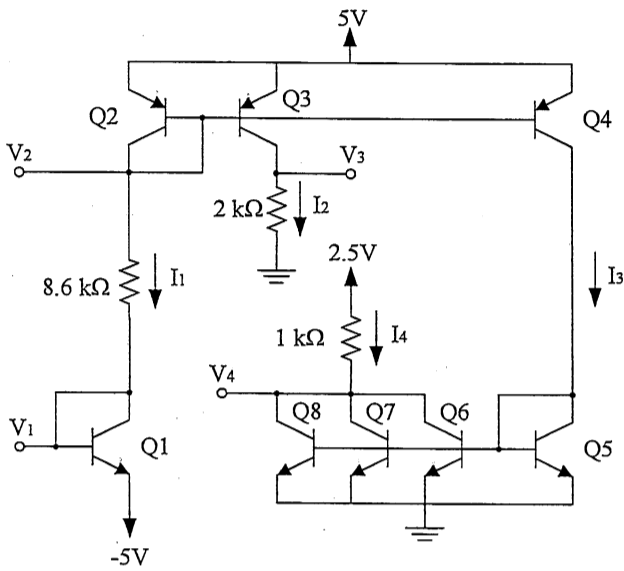


Fig.1

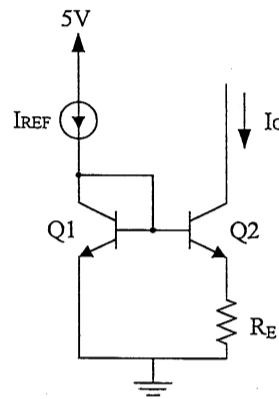


Fig.2

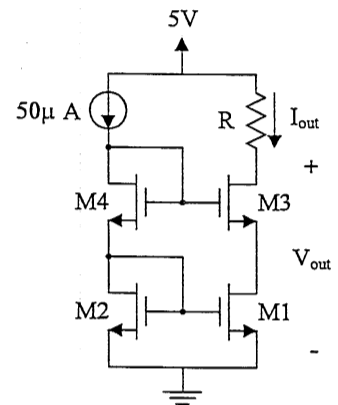


Fig.3

2. (16%) Consider the Widlar current source shown in Fig. 2 for generating a constant current $I_O=100\mu A$ with $I_{REF}=1mA$.

(a) Determine the value of R_E .

(b) Estimate the output resistance for $\beta=100$ and $V_A=100V$.

3. (16%) Consider the cascode current mirror as shown in Fig. 3, where all the transistors are identical with $\mu_n C_{ox}=160\mu A/V^2$, $V_{tn}=0.5 V$ and $W/L = 10$.

(a) What is the maximum resistance R for the cascode current mirror shown in the figure without any transistors entering the triode region? (Neglect the body effect and the channel length modulation effect of the transistors.)

(b) Estimate the output resistance seen into transistors M3, where $\lambda=0.1 V^{-1}$.

4. (16%) Consider the circuit shown in Fig. 4.

(a) Find the feedback factor β .

(b) Assuming the opamp is ideal, find the closed-loop gain v_O/v_I . If $v_I=0.5V$, determine v_n .

(c) Repeat part (b), if the opamp gain is $A=500$.

(d) If the op amp is nonideal, and has a low-frequency gain of 500 and a single-pole rolloff at 5 kHz, determine bandwidth of the feedback circuit.

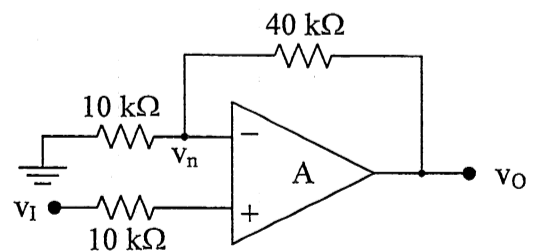


Fig. 4

<背面繼續>

大同大學 101 學年度研究所碩士班入學考試試題

考試科目：電子學

所別：電機工程研究所

第 2/2 頁

註：本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

< 接前頁 >

5. (20%) Consider the two-stage amplifier shown in Fig. 5, where $\mu_n C_{ox} = 160 \mu A/V^2$, $\mu_p C_{ox} = 64 \mu A/V^2$, $V_{tn} = |V_{tp}| = 0.5V$, $\lambda_n = \lambda_p = 0.1 V^{-1}$. All the transistors have a channel length of $1 \mu m$, and the channel widths are indicated in the figure.
- Determine the transistor currents $I_{D1} - I_{D10}$.
 - Find the low-frequency gain for the first and second stages (v_{o1}/v_d and v_{o2}/v_{o1}), respectively. v_d is the voltage difference between v_{IN+} and v_{IN-} .
 - Neglecting the internal capacitances, estimate the pole due to the compensation capacitor C_c .

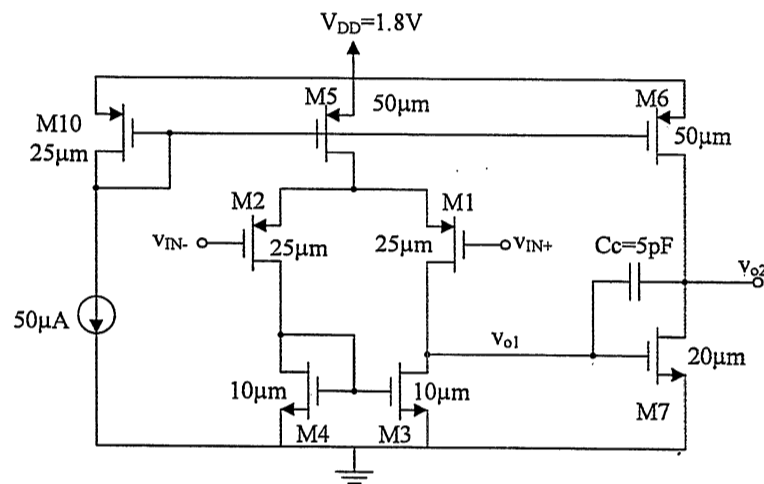


Fig.5

6. (16%) The circuits of Fig.6 show different implementations of an inverter. Neglect the body effect. ($V_{tn} = |V_{tp}| = 0.5V$)
- Determine V_{OH} (output at $V_{in} = 0V$) of the 3 inverters.
 - Calculate the static power consumption at $V_{in} = 0V$.
 - V_{OL} (output at $V_{in} = V_{DD}$) of which circuit(s) is $0V$?
 - Determine the static power consumption at $V_{in} = 1.8V$. ($\beta_n = 4 \times \beta_p = 320 \mu A/V^2$)
 - Which circuit(s) is(are) a ratio circuit(s)? (i.e. the proper functionality of the circuit depends on the size of the devices.)

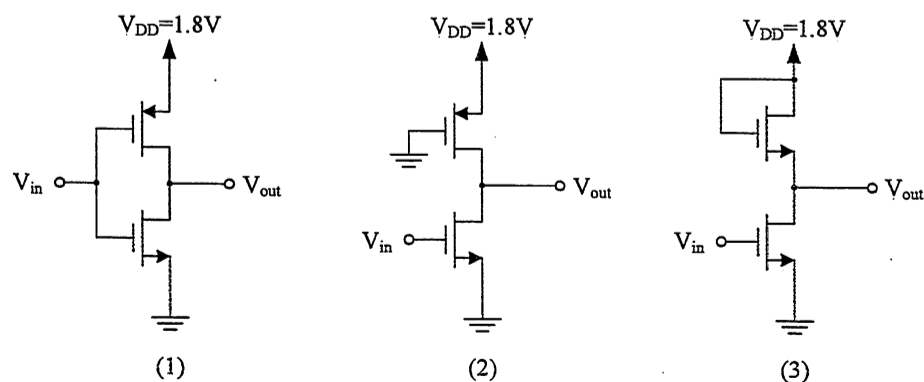


Fig.6