大同大學 102 學年度研究所碩士班入學考試試題

考試科目：電子學　　所別：電機工程研究所　　

註：本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 不可以使用計算器。

1. (a). Derive the transfer function $T(s)=V_{O2}/V_{O1}$ and find 3dB frequency ω_p. (6%)(Fig. P1)

(b). $V_I(t) = V_P \sin \omega t$, draw the V_{o1} vs ωt plot for $0 \le \omega t \le 2\pi$, **derive the average value of $V_{o1}(t)$.(7%)**

(c). If $\omega_p << \omega$, write an expression for the output $V_{o2}(t)$.(3%)

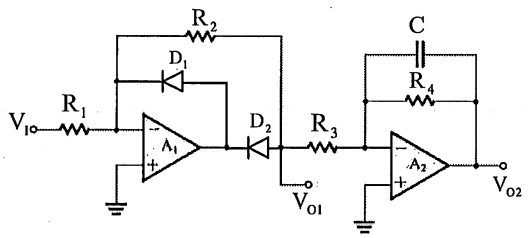

Fig. P1

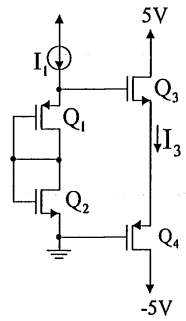

Fig. P2

2. (a). For the circuit in Fig. P2, derive $\frac{I_1}{I_3}$ in term of K_1, K_2, K_3 and K_4, where $K_i=\frac{1}{2}\mu C_{ox} W/L$ corresponding to the MOS Q_i with $V_{tn} = -V_{tp}$. (Assume Q_3 and Q_4 are in satutration.) (8%)

(b). If $K_1=K_2$, $K_3=K_4=16\ K_1$, find the required value of I_1 to yield a bias current in Q_3 and Q_4 of 1.6mA.(3%)

3. CMOS amplifier, $\mu_n C_{ox}$ =110 μA/V², $\mu_p C_{ox}$ =50 μA/V², $V_{tn} = -V_{tp}$=0.7 V, $|\lambda| = 1/|V_A| = 0.04V^{-1}$ for both n/pMOS, I_R=30μA, $V_{DD}=V_{SS}$=2.5 V, Cc =3 PF, let $v_1 = -v_{id}/2$, $v_2 = v_{id}/2$.

MOS	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
W/L(μm/μm)	3/1	3/1	15/1	15/1	5/1	5/1	15/1	90/1

(a). Calculate the value of R_R . (6%).

(b). Determine the MOS dc currents I_{D2} and I_{D8}.(4%)

(c).Calculate the low frequency voltage gain A_1, A_2, for the 1st and 2nd stage. (14%)

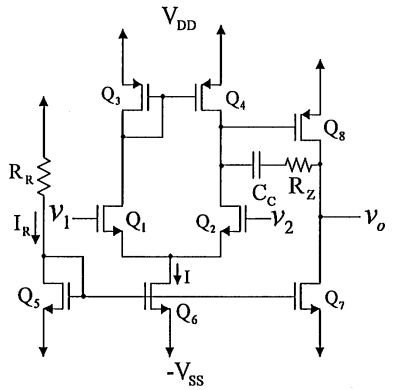

Fig. P3

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考試科目：電子學　　所別：電機工程研究所　　第2/2 頁

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4. For the BJT amplifier,all the current sources are ideal,for all BJTs β=100, $r_o=\infty$, let $v^+=v_{id}/2$, $v^-=-v_{id}/2$, $R_L=10k\Omega$,

(a). For inputs grounded and output held at 0V find the dc collector current I_{C2} (Q_2).(2%)

(b). Draw the small-signal circuit and calculate low frequency voltage gain, $A=v_o/v_{id}$ (12%)

(c). Find the value of C_C to obtain a 3-dB frequency of 100 Hz ? (4%)

(d). Calculate the unity gain frequency f_t in Hz. (4%)

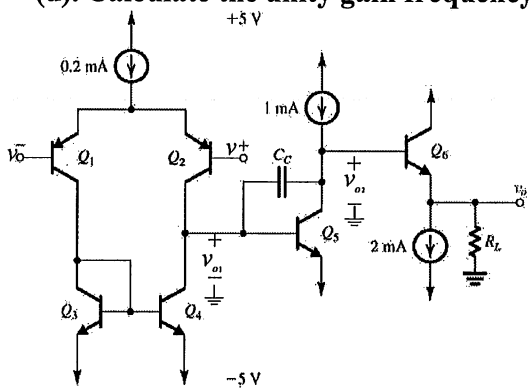

Fig. P4

5. (a). Draw the CMOS inverter circuit, define $K_R=\frac{\mu_n C_{ox}(W/L)_n}{\mu_p C_{ox}(W/L)_p}$, V_{tn} and $V_{tp}(<0)$ are the threshold of n/pMOS respectively, derive an expression for the switching threshold voltage, V_{th}.(12%)

(b). If K_R increases, will the v_{th} increase or decrease? Verify your answer. (4%)

6. (a). Draw the CMOS circuit to implement $Y=\overline{A(B+C)}$ (5%)

(just use A, B and C as inputs and use minimum number of MOS transistors)

(b). Construt the truth table for the CMOS circuit and determine the logic function Y=? (6%)

(Fig. P6(b))

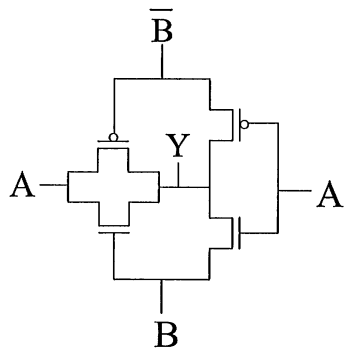

Fig. p6(b)