大同大學 103 學年度研究所碩士班入學考試試題

考試科目:電子學　　所別:電機工程研究所　　

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 不可以使用計算器。

1. For the circuit in Fig. 1, $V_{DD} = 2\,\text{V}$, $\mu_n c_{ox} = 160\,\mu\text{A/V}^2$, $V_{tn1} = V_{tn2} = 0.5\,\text{V}$, $(W/L)_1 = 4(W/L)_2 = 4$, $R_1 = 12.5\,\text{k}\Omega$ and transistors M_1 and M_2 operate in saturation region.
   (a) (5%) Give the value of I_R.
   (b) (5%) Find the value of R_2 if $I_o = 5\mu\text{A}$.
   (c) (6%) Derive the expression of R_o in term of g_{m2}, r_{o2} and R_2.
   (d) (4%) Give the value of the output resistance R_o if $|V_A| = 5\text{V}$.

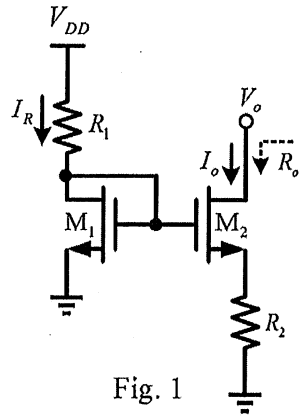

Fig. 1

2. For the circuit in Fig. 2, the opamp has an open loop gain A = 40 dB, an infinite input resistance and a zero output resistance, $R_1 = R_3 = 10\,\text{K}\Omega$, $R_2 = 90\,\text{K}\Omega$, the capacitor C = 10 μF is only considered in part (c), and the resistor R_L is only considered in part (d).
   (a) (3%) Identify the feedback topology and give the feedback factor β.
   (b) (5%) Find the dc closed loop gain v_o/v_i.
   (c) (9%) Find the zero and pole of the transfer function $v_o(s)/v_i(s)$ when the capacitor C is parallel connected to the resistor R_2.
   (d) (5%) Find the minimum value of R_L if $v_i = 1\,\text{V}$ and $i_{O,max} = 50\,\text{mA}$ is given.

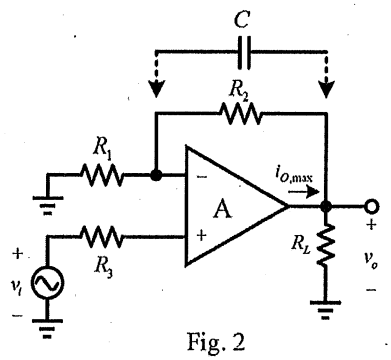

Fig. 2

3. Assume all diodes in Fig. 3 have 1 V voltage drop when they conduct.
   (a) (10%) Derive the relationship of V_O and V_I for the circuit ing Fig. 3a and Fig. 3b.
   (b) (8%) Draw the transfer curve V_O vs V_I and indicate the voltages at the breaking points when $-10\text{V} \le V_I \le 10\text{V}$ is given.

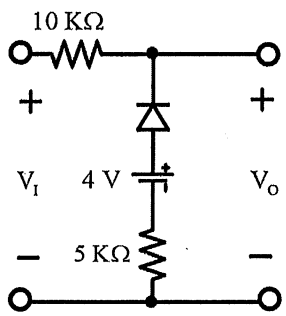

Fig. 3a

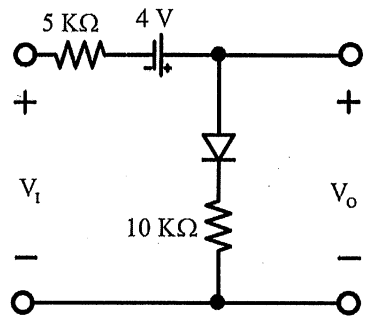

Fig. 3b

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4. (a) (5%) Find the logic function F for the circuit in Fig. 4.
   (b) (5%) Give a circuit that performs the Boolean function $F = \overline{A \oplus B}$ and is implemented in static CMOS gate.

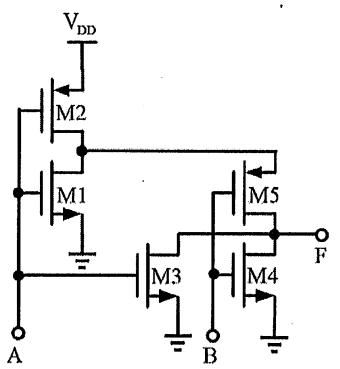

Fig. 4

5. The circuits in Fig. 5 demonstrate different implementations of an inverter. Assume PMOS and NMOS have same parameters, ie., $\mu_n c_{ox}(W/L)_n = \mu_p c_{ox}(W/L)_p$, $V_{tn} = |V_{tp}| = V_t$.
   (a) (2%) Which circuit consumes static power when $V_I = V_{DD}$?
   (b) (6%) Give the V_{OH} (in terms of V_{DD} and V_t) of each circuit.
   (c) (2%) Which circuit has V_{OL} that equals to 0 V?
   (d) (4%) Find the voltage of V_O (in terms of V_{DD} and V_t) in Fig. 5(b) when $V_I = V_{DD}$.

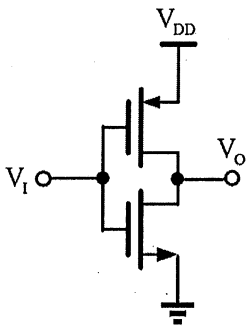

Fig. 5a

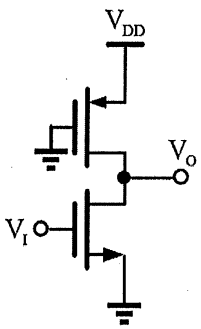

Fig. 5b

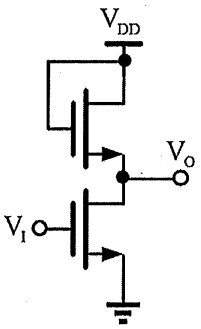

Fig. 5c

6. For the circuit in Fig. 6, transistors Q1 and Q2 are identical and have $\beta = 100$, thermal voltage $V_T = 25$ mV, $|V_A| = 10$ V.
   (a) (5%) Find the input resistance R_i.
   (b) (5%) Find the output resistance R_o when $v_i = 0$.
   (c) (6%) Find the global voltage gain $G_v = v_o/v_{sig}$ when $R_{sig} = 0.1\ \text{k}\Omega$ and $R_L = 2\ \text{k}\Omega$.

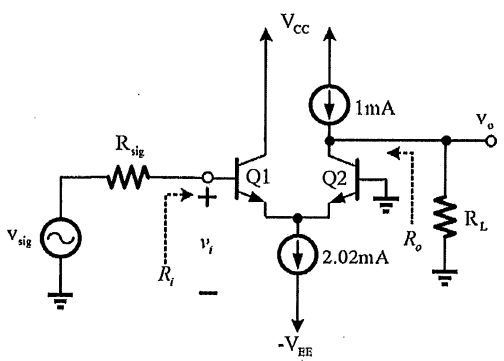

Fig. 6