大同大學 九十 學年度研究所碩士班入學考試試題

考試科目：**計算機組織**　　所別：**電機工程研究所**　　第1/1頁

註:本次考試　不可以參考自己的書籍及筆記；　不可以使用字典；　不可以使用計算器。

1. Design a logic circuit to implement a counter with the following binary sequence : 0,1,3,7,6,4 and repeat. (12%)
2. Consider the calculation of $y = A_1 \times X_1 + A_2 \times X_2 + A_3 \times X_3$. The fixed coefficients $A_1 = 0.72$, $A_2 = -0.3$, and $A_3 = 0.95$. Each X_k is a 2's complement binary number scaled such that $|X_k| < 1$ and is expressed as $X_k = -b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n}$ where N=8, b_{kn} are the bits, 0 or 1, and b_{k0} is the sign bit. Use an 8-word ROM and an adder/subtractor to construct a circuit to compute y when X_1, X_2 and X_3 are bit-serially input. The operation of the circuit and the content of 8-word ROM should be described. (12%)
3. (a) Please describe what the nonrestoring division is ?
   (b) Try to compare the computing complexity of nonrestoring division and that of restoring divisioin ? (12%)
4. Suppose a computing task can be divided into k subtasks and then accomplished by a pipeline of k stages. Try to evaluate the speedup of the pipelined operation versus the sequential operation (non-pipelined operation) as n tasks are executed, where each stage of the pipeline is assumed taking τ time units to finish the subtask and neglecting the staging delay. (16%)
5. (a) Try to illustrate how a floating-point adder performs in 4 functional blocks.
   (b) Try to implement (a) in pipeline architecture.
   (c) What is the advantage of (b), and what is its overhead ? (12%)
6. The logical address space in a computer system consists of 128 segments. Each segment can have up to 32 pages of 4K words. Physical memory consists of 4K blocks of 4K words. Show formats of logical and physical addresses. (12%)
7. A digital computer has a memory unit with 24 bits per word. The instruction set consists of 150 different operations. There is only one type of instruction format with an operation code part and an address part. Each instruction is stored in one word of memory.
   (a) How many bits are needed for the operation code part?
   (b) How many bits are left for the address part of the instruction?
   (c) How many words are there in the memory and what must be the memory size?
   (d) What is the largest unsigned binary number that can be accommodated in one word of memory? (12%)
8. How many bus arbitration schemes are there? Describe at least three different schemes. (12%)