大同大學 九十 學年度研究所碩士班入學考試試題

考試科目：電子學　　所別：電機工程研究所　　第 2 頁

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

1. (a)For an abrupt PN junction the depletion-region width as a function of voltage is given by $W=\left[\frac{2\varepsilon_{si}}{q}(\frac{1}{N_A}+\frac{1}{N_D})(V_0-V)\right]^{\frac{1}{2}}$, where V_0 is the built-in voltage, ε_{si} is the permittivity of Si. Derive the junction capacitance $c=c_0/\sqrt{1-V/V_0}$, define the c_0. (5%)

   (b) If $N_A=10^{18}cm^{-3}$, $N_D=10^{15}cm^{-3}$ and PN junction area $A=6\times10^{-4}cm^2$, calculate the junction capacitance for reverse-biased of 10 Volts. (the dielectric constant of Si :11.9, intrinsic carrier concentration of Si: $n_i=1.5\times10^{10}cm^{-3}$, permittivity of vacuum: $8.85\times10^{-14}F/cm$, T=27°C) (8%)
2. A logic gate has a delay-power product of 1 pJ. The gate power dissipation is 1 mW. What is the gate switching time? (4%)
3. For a CMOS gate shown in fig.P3, derive the transition points of (a) $M_2: V_{out}=V_{in}-V_{tp}$ (b) M_1: $V_{out}=V_{in}-V_{tn}$ where V_{tn} and V_{tp} are the threshold voltage of NMOS and PMOS respectively. (12%)

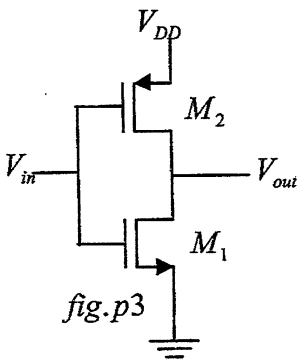

fig.p3

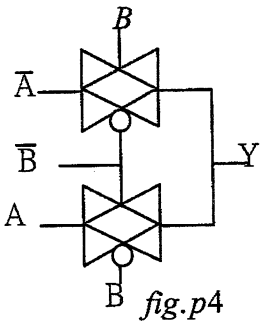

fig.p4

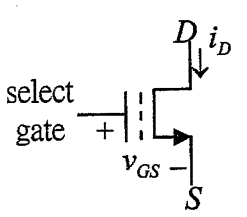

fig.p5

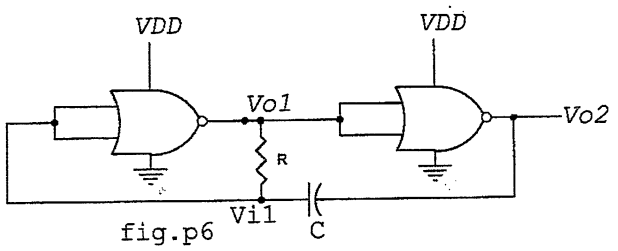

fig.p6

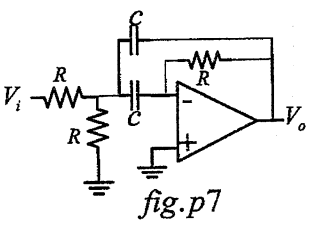

fig.p7

4. Please write down the output function Y in terms of inputs in the logic circuit as shown in fig.p4. (5%)
5. The floating-gate transistor used as an EPROM cell shown in fig.p5, please sketch i_D-v_{GS} curve. (6%)

<背面繼續>

大同大學 九十 學年度研究所碩士班入學考試試題

考試科目：電子學　　所別：電機工程研究所　　第 2 頁

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

6. Sketch the timing waveforms; V_{o1}, V_{o2} and V_{I1} for the circuit shown in fig.p6. (12%)
7. Consider the circuit shown in fig.p7.
   (a) Assuming the opamp is ideal, derive the transfer function T(s). (12%)
   (b) Determine the type of the filter. (3%)
8. Consider the cascode current mirror as shown in fig.p8 , where all the transistors are identical with $\mu_n C_{ox}$=100μA/V^2, V_{tn}=0.8 V and W/L =8.
   (a) What is the maximum resistance R for the cascode current mirror shown in the figure without any transistors entering the triode region? (Neglect the body effect and the channel length modulation effect of the transistors.) (5%)
   (b) Estimate the output resistance seen into transistors M3, where λ=0.025 V^{-1}. (5%)

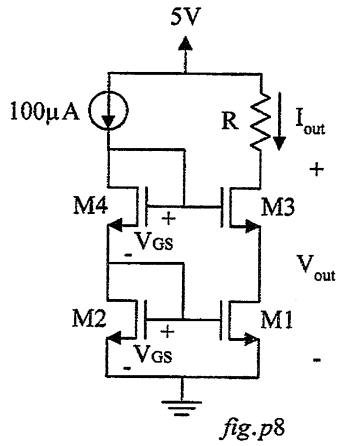

fig.p8

9. For the circuit shown in fig.p9 , the parameters for the NPN transistor are $V_{BE(on)}$=0.7V, β=120 and V_A=100V. The parameters for the NMOS transistor are $\mu_n C_{ox}$=100μA/V^2, V_{tn}=0.8 V and W/L =8. (V_T=25mV)
   (a) If the bias current of the NMOS transistor is set to be 100μA, find the resistance for Rs. (Neglect the body effect and the channel length modulation effect of the NMOS transistor.) (5%)
   (b) Calculate the small-signal midband gain $A_v=v_{o2}/v_i$. (5%)
   (c) Estimate the upper 3-dB frequency (in Hz). (Neglect the internal capacitors of the transistors.) (3%)
   (d) Determine the pole and zero introduced by C_{C1}. (5%)
   (e) If a capacitor of 100pF is connected between v_{o1} and v_{o2}, estimate the upper 3-dB frequency again. (5%)

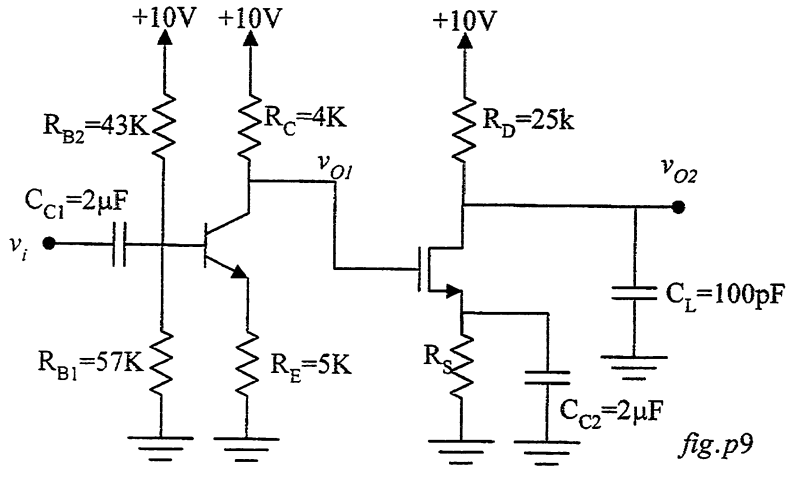

fig.p9