大同大學九十二學年度研究所碩士班入學考試試題

考試科目:電子學　　所別:電機工程研究所　　

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

1. **(8%)(a). As shown in Fig. p1, initially $V_O(t=0)=0$, set $V_{in}=V_{DD}$ at t=0, show that**

$V_O(t)=V_f[\frac{t/\tau}{1+(t/\tau)}]$, **define V_f and τ in terms of $V_{DD}, C, V_t, K_n(=\mu_n C_{OX} W/L)$ etc..**

(b). What is the steady state output voltage V_f in terms of parameters above.

2. **(6%) Given nMOS threshold voltage $V_t=V_{t0}+\frac{\sqrt{2q\varepsilon_{Si}N_A}}{C_{OX}}\left(\sqrt{|2\phi_f|+V_{SB}}-\sqrt{|2\phi_f|}\right)$, derive**

$g_{mb}=\chi g_m$, where g_m and g_{mb} are the transconductance and body transconductance respectively, define the χ.

3. **(10%) For the ideal opamp.circuit shown in Fig. p3 derive an expression for the transfer function Vo/Vi. Find expressions for the magnitude and phase of the response.**

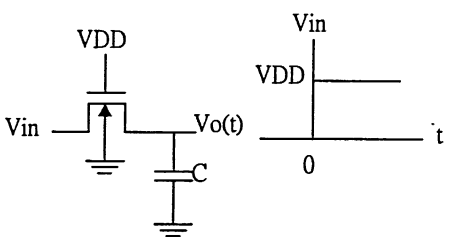

Fig. p1

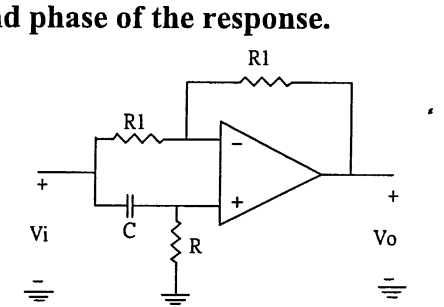

Fig. p3

4. **(20%) Consider the cascode gain stage of Fig. p4, where $\mu_n C_{ox}=2.5\times\mu_p C_{ox}=100\mu A/V^2$, $V_{tn}=-V_{tp}=0.7V$, $\lambda_n=\lambda_p=0.025\ V^{-1}$, $(W/L)_1=(W/L)_2=(W/L)_3=(W/L)_4=50$, $(W/L)_5=(W/L)_6=(W/L)_7=(W/L)_8=20$ and $(W/L)_9=(W/L)_{10}=100$.**

(a). Find the value for R_B.

(b). Estimate the low-frequency differential voltage gain (in dB). (Neglect the body effect.)

(c). Estimate –3dB bandwidth and unity-gain bandwidth.

(d). Calculate the input common-mode range.

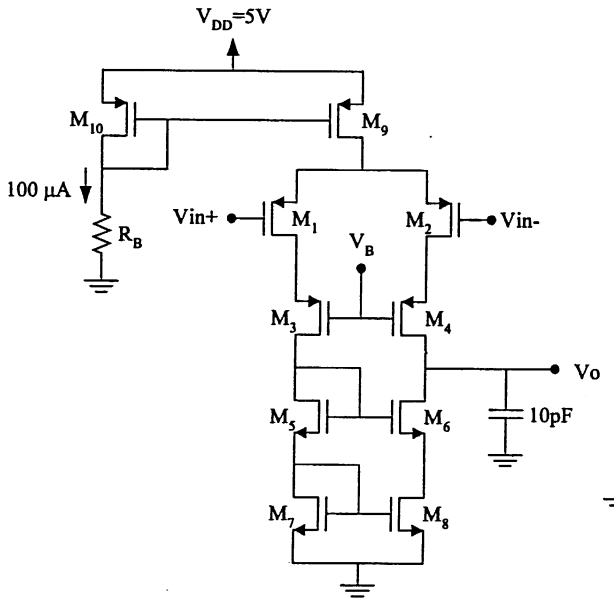

Fig. p4

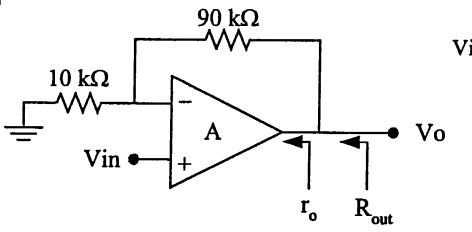

Fig. p5

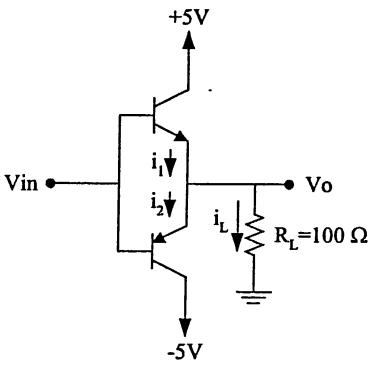

Fig.p6

5. **(10%) For the circuit shown in Fig. p5, the opamp has an open-loop gain (A) of 10^4 and output resistance ro=1kΩ.**

(a). Find the voltage gain (Vo/Vin) and output resistance (R_{out}) for the closed-loop circuit.

(b). If the bandwidth of the opamp is 100 Hz, what is the bandwidth of the closed-loop circuit?

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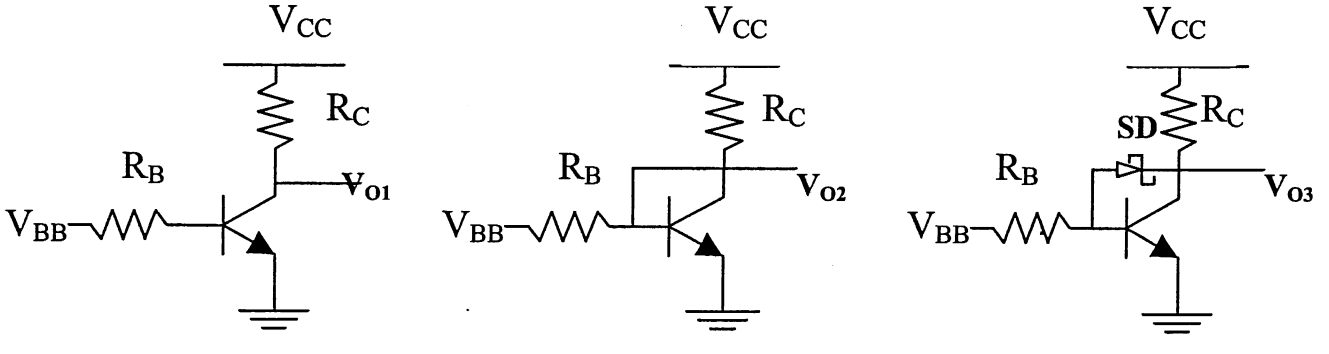
6. (10%) Consider a class-B output as shown in Fig.p6 with a 1kHz sine-wave input of 2.5V peak.

(a). Assuming $|V_{BE}|$=0.7V, draw the waveforms for Vin and currents i_1, i_2 and i_L.

(b). Calculate the root-mean-square value for i_1.

7. (12%) (a) Determine the transistors operated in which region (linear, sturation, or cutoff region) with $R_C = 1\ K\Omega$, $R_B = 4.3\ K\Omega$, $V_{CC} = V_{BB} = 5$ volts, $\beta_F = 50$, $V_{BE(on)} = 0.7$ volts and $V_{CE(sat)} = 0$ volts, $V_{SD} = 0.4$ volts.

(b) Determine the output voltage of each circuit below.



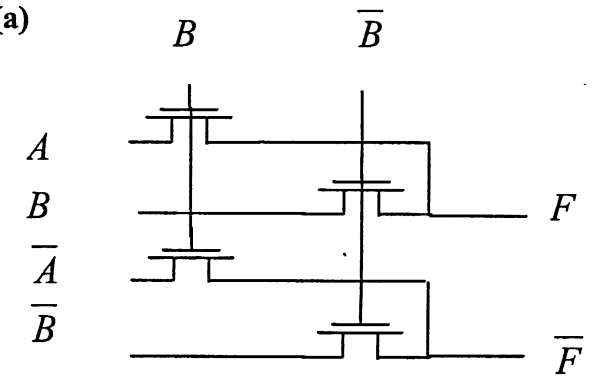
8. (12%)An inverter drives an identical inverter with the propagation delay of $t_{pinv} = t_{PHL} = t_{PLH}$, assume the minimum size of transistors are $(W/L)_P = 2, (W/L)_N = 2$.

(a). Draw the conventional CMOS schematic digram of the logic function F=NOT((A+B)C+DE) with the minimum delay(consider the diffusion capacitance effect).

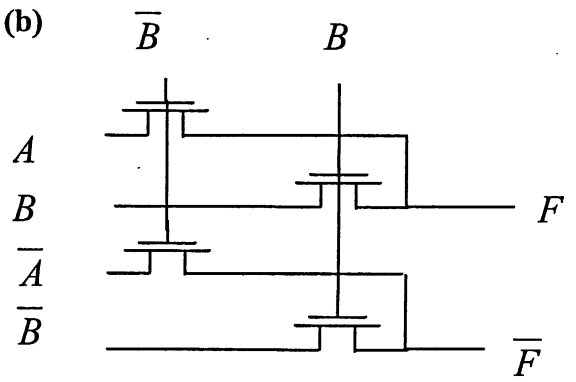
(b). If the sizes of all transistors are same as the inverter, find the propagation delay(t_{PHL}, t_{PLH}) of this logic circuit in the worst case.

9. (12 %) Determine the logic fuction in the following circuits.

(a)



(b)



(c)