大同大學 九十三 學年度研究所碩士班入學考試試題

考試科目:電子學　　所別:電機工程研究所　　

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

1. **(10%)For the circuit in Fig. P1, derive the output waveform $v_O(t)$ and sketch $v_O(t)$ vs t plot for the input shown. Label the most positive and most negative output levels. Assume $RC >> T$,ideal diode.**

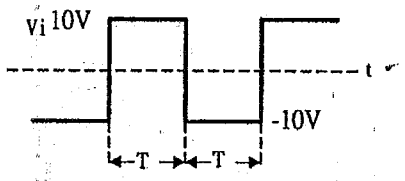
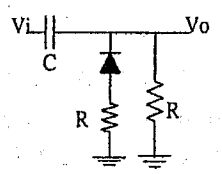


Fig. P1



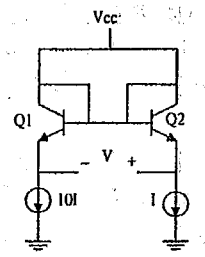


Fig. P2

2. **(6%)In Fig. P2, two identical BJTs are biased in the forward-active region by current sources with 10:1ratio. Caculate the the voltage $V_$ at temperature T=25° C .**

3. **(12%)A feedback amplifier for which the open-loop transfer function is given by** $A(s)=\dfrac{10^3}{(1+\frac{s}{10^4})(1+\frac{s}{10^5})^2}$**,let the feedback factor β be a constant independent of frequency.**

   (a). Find the frequency ϖ_π at which the phase shift is –180°

   (b). Calculate the critical value β_{max} which will keep the amplifier stable.

4. **(18%) Consider the two-stage amplifier shown in Fig. P4, where μ_nC_{ox}=2.5×μ_pC_{ox} =100μA/V², V_{tn}=V_{tp}=0.6V, λ_n=λ_p =0.04 V⁻¹. All the transistors have a channel length of 1μm, and the channel widths are indicated in the figure.**

   (a) Find the low-frequency gain for the first and second stages (v_{o1}/v_d and v_{o2}/v_{o1}), respectively.

   (b) Neglecting the internal capacitances, estimate the pole and zero due to the compensation capacitor Cc.

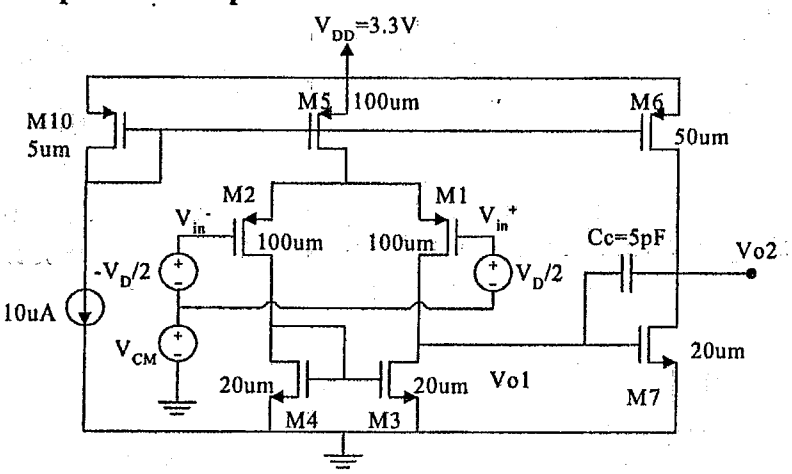


Fig. P4

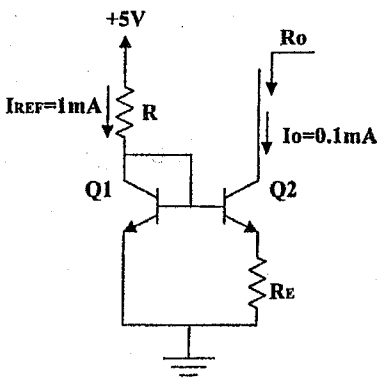


Fig. P5

5. **(12%) Assuming transistors Q1 and Q2 are matched, estimate R_E and the output resistance R_o for the Wildlar current source shown in Fig.P5, where V_T=26mV, β=120 and V_A=100V.**

〈背面繼續〉

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6. **(8%) Consider a Miller integrator shown in Fig. P6, and its output is initially zero. Sketch the output waveform for the circuit when fed with a string of pulses of 20μs duration and 2V amplitude rising from 0V. How many pulses are required for an output voltage change of 1V?**

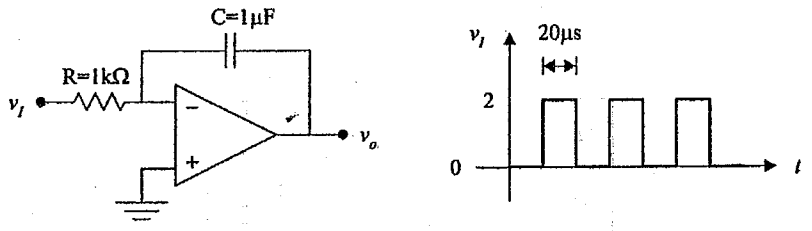
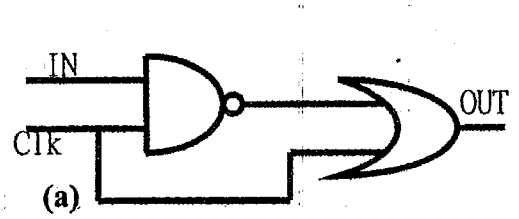
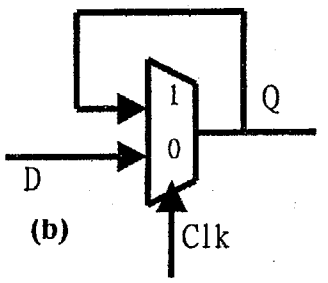
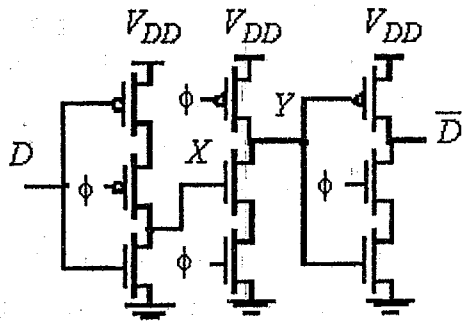


Fig. P6

7. **(12%)Determine the following gates or circuits are belong to positive or negative egdge trigger, why? Describe briefly.**







8. **(12%) In the MOS inverters, $(W/L)_{pinv}$ and $(W/L)_{ninv}$ are the size of the PMOS and NMOS respectively. Describe the relationship between $(W/L)_{pinv}$ and $(W/L)_{ninv}$ (>,< or =) required to meet the following conditions.**
   (a). if we need noise margin high (NMH) equals to noise margin low (NML)
   (b). if we need the propagation delay $t_{PHL} > t_{PLH}$.
   (c). if we need the switching threshold voltage (V_M) is less thsn half of power supply V_{DD}, i.e. $V_M < (1/2)V_{DD}$.
   You must describe why it is briefly.

9. **(10%)Using two stage buffer to drive an external capacitor C_{ext} of 2.5 pF, If the first stage inverter has the input capacitor , C_g, of 100fF with the minimum size (i.e. W/L = 1) transistors, and the size of the second stage inverter is f.**
   (a). Find the size f to optimumize the propagation delay and find the delay in termsof t_{p0} which is the delay of an inverter to drive a same size inverter.
   (b). If we need the minimum energy, what is the size f? And find the energy with V_{DD} = 5 Volts.