大同大學 九十四 學年度研究所碩士班入學考試試題

考試科目:電子學　　所別:電機工程研究所　　

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

1. (12%) In Fig. 1, $\mu C_{ox}(W/L) = 1mA/V^2$ for both NMOS and PMOS, $V_{tn} = -V_{tp} = 1V$ and neglect the body effect. Calculate I_{Dn}, I_{Dp} and V_O when $V_I = 2.5V, -2.5V$.

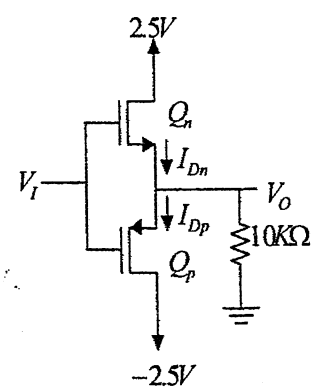

Fig. 1

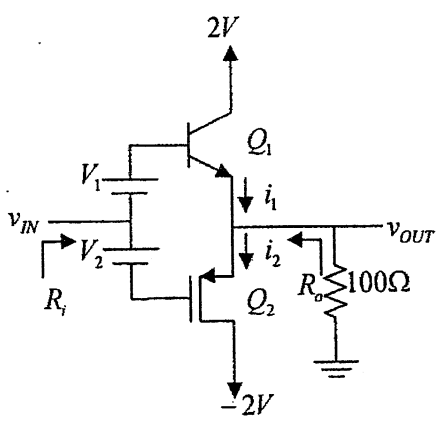

Fig. 2

2. (22%) Refer to Fig. 2, neglect the body effect, the channel modulation, and the Early effect. The parameters for BJT are $\beta = 100$ and $I_S = 10^{-14}A$, for PMOS, $\mu_p C_{ox} = 50\mu A/V^2$, $W/L = 100$ and $V_{tp} = -0.7V$.

(a) In case $v_{IN} = 0$, calculate the value of V_1 and V_2 which will keep $i_1 = i_2 = 100\mu A$.

(b) With V_1 and V_2 as calculated as in part (a), apply an ideal source v_{IN}, sketch the small signal equivalent circuit and calculate the input resistance R_i, output resistance R_o and small signal voltage gain.

3. (8%) For the feedback circuit shown in Fig.3, the amplifier has a low-frequency gain of 2000 and a single-pole rolloff at 1 kHz. If β is 0.5, find the low-frequency gain and the bandwidth of the feedback circuit.

4. (15%) Consider the differential pair shown in Fig. 4, where W/L values are given in the figure, $\mu_p C_{ox}$ =25μA/V^2 and V_{tp}= −0.6V. Neglect the channel length modulation effect.

(a) Find the minimum value of v_{id} that causes M1 to conduct the entire current I.

(b) Find the equivalent small-signal transconductance for the differential pair (input: v_{id}, and ouput: $i_{D1}-i_{D2}$).

(c) What is the lowest value of V_{CM} (v_{id} =0) for which M1 and M2 remain in saturation?

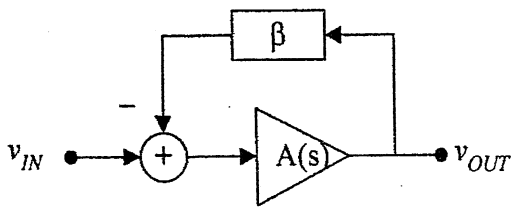

Fig. 3

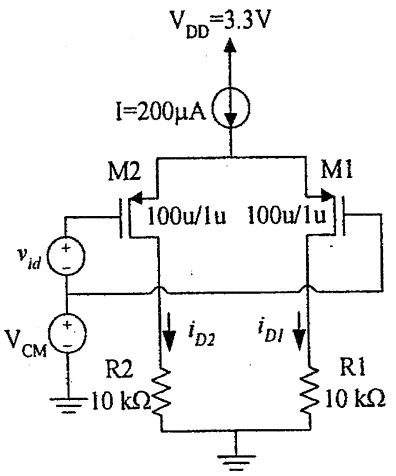

Fig. 4

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5. (10%) Consider the common-source amplifier shown in Fig. 5, where W/L values are given in the figure, $\mu_n C_{ox}=2.5\times\mu_p C_{ox}$ $=100\mu A/V^2$, $V_{tn}=-V_{tp}=0.6V$, $\lambda n=0.04V^{-1}$ and $\lambda p=0.08V^{-1}$.

   (a) Estimate the low-frequency voltage gain, where V_{IN} is given such that all transistors are in the saturation region.

   (b) If $C_{gd1}=5fF$ and $C_{gs1}=80fF$, estimate the total capacitance seen by R_{IN}.

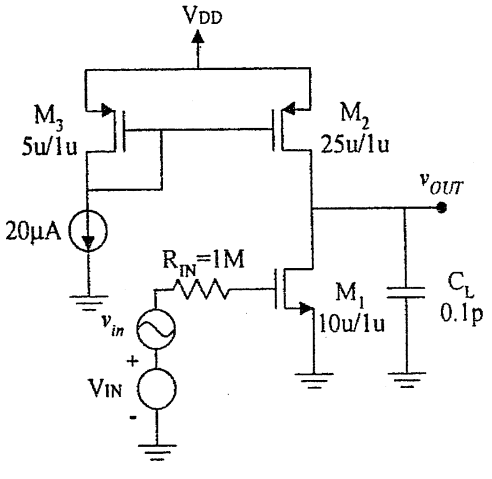

Fig. 5

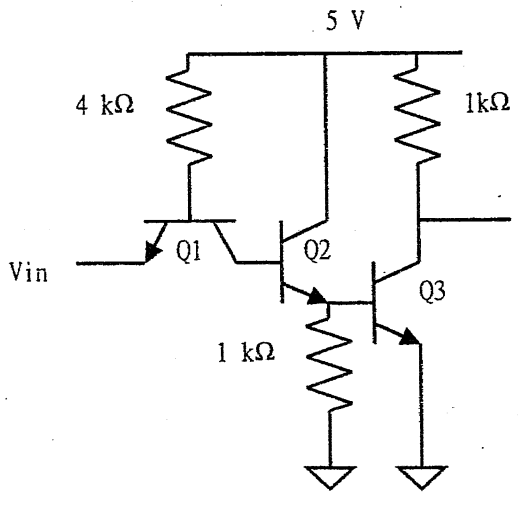

Fig. 6

6. (18%) Determine the mode of operation (cutoff, active or saturated mode) for each transistor in the circuit shown in Fig. 6 when (a)Vin=0V,(b)Vin=5V. And assume $\beta_F = 100$, $\beta_R=0.5$, $V_{BE(ON)}=0.7V$, $V_{BE(sat)}=0.8V$ and $V_{CE(sat)}=0.1V$. Why? Descript it briefly.

7. (15%) (a) Draw a CMOS inverter with $V_{DD} = 5V$, where $\mu_n C_{ox} =115\mu A/V^2$, $\mu_p C_{ox} =30\mu A/V^2$, and $V_{tn}=|V_{tp}|=1V$.

   (b) Assuming the W/L = 1 of the NMOS device, design the inverter with a 2.5V logic switching threshold voltage. What is the W/L of the PMOS device?

   (c) Draw the curve of current ($I_{DN}=|I_{DP}|$) vs $V_{in,}$ as V_{in} from 0V to 5V. Label the important points, like the voltages of start point and end point of the current flow.

   (d) When the inverter with the load capacitor C_L, how does change the C_L affect the current curve in part (c)?