1. (12%) Consider the circuit of Fig. 1. For (a). v_I =1 V and (b). v_I = -1 V, calculate the voltages at v_O and v_A. Assume that the op amp is ideal and its output saturates at ± 12 V, the diode has a 0.7 V drop at 1 mA current, and its voltage drop changes by 0.1 V per decade of current change.

2. (12%) Refer to Fig. 2, the op amp has open-loop gain (A) of 10^3, the 3dB bandwidth (f_H) of 100 Hz and output resistance $R_O = 10^5 \Omega$. Find the voltage gain (V_o/V_i), 3dB bandwidth (f_{Hf}) and output resistance (R_{Of}) of the closed-loop circuit.

3. (10%) For the circuit in Fig. 3, neglect base currents and derive I_3/I_1 in term of I_{S1}, I_{S2}, I_{S3} and I_{S4}, where I_{Si} is the saturation current corresponding to the BJT Q_i.

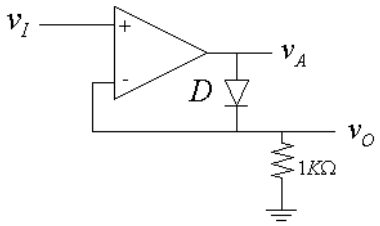

Fig. 1

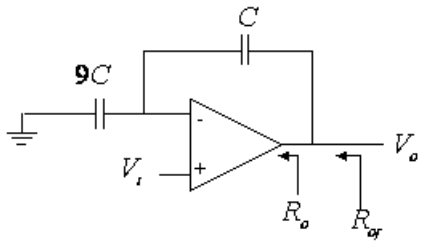

Fig. 2

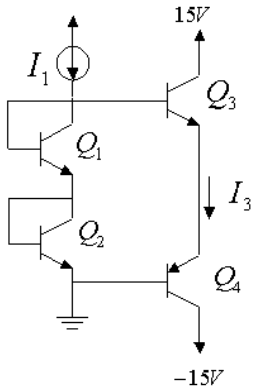

Fig. 3

4. (17%) The small-signal equivalent circuit of a two-stage amplifier is shown in Fig.4 , where R_{in}=1MΩ, Cc=1μF, g_{m1}=100μA/V^2, g_{m2}=125μA/V^2, R_1=200kΩ, R_2=250kΩ, C_1=0.5pF and C_2=2.5pF.
   (a) Determine the midband gain (in dB).
   (b) If a compensation capacitor (2pF) is added between nodes 1 and 2, estimate the dominant pole frequency (in Hz).
   (c) Roughly sketch the magnitude response of the amplifier gain (v_o/v_{in}) after compensation, and indicate the -3dB frequencies (in Hz) in your plot.
   (d) Find the zero results from the compensation capacitor. Is the zero located in the right-half or the left-half plane?

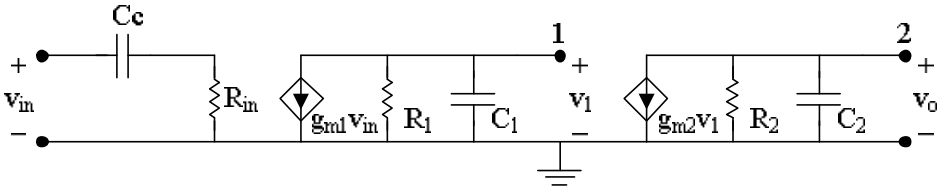

Fig. 4

5. (17%) Consider the circuit shown in Fig. 5, where R_G=1MΩ, R_{sig}=200kΩ, R_L=10kΩ, V_{DD}= −V_{SS}=5V, m_nC_{ox}=100μA/V^2, $(W/L)_1$= $(W/L)_2$=20 and V_{tn}=0.6V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest. Neglect the body effect.

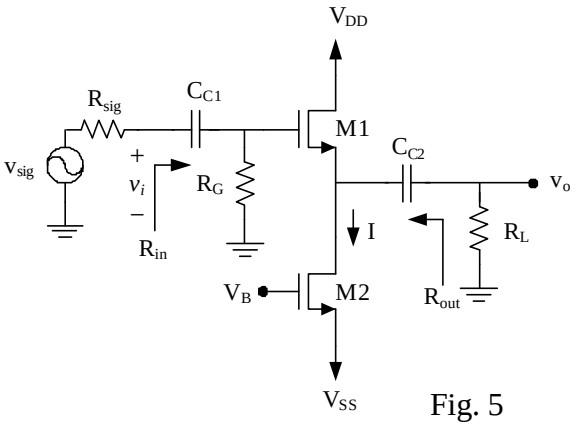

Fig. 5

(a) Transistor M2 is used as a current source to provide I=1mA. Find the value for V_B, and the minimum drain voltage for M2 to act as a current source.
(b) Find R_{out} and A_v (v_o/v_i). (λ =0.04 V^{-1})
(c) Find R_{in}, and the overall small-signal voltage gain G_v (v_o/v_{sig}).
(d) If the bodies of the two transistors are tied together, which transistor suffers from body effect?

6. (16%) The circuits of Fig. 6 show different implementations of an inverter whose output is connected to a capacitor. Assume V_{tn}= 0.4 V for 0.13 μm technology.

(a) Which one of the circuits consumes static power when the input is high? Why?
(b) Which one of the circuits consumes static power when the input is low? Why?
(c) V_{OH} of which circuit(s) is 1.2 V? Why?
(d) V_{OL} of which circuit(s) is 0 V? Why?
(e) V_{OH} or V_{OL} of which circuit(s) depends on the size of the devices? (i.e. which circuit(s) is(are) a ratio circuit(s)?)

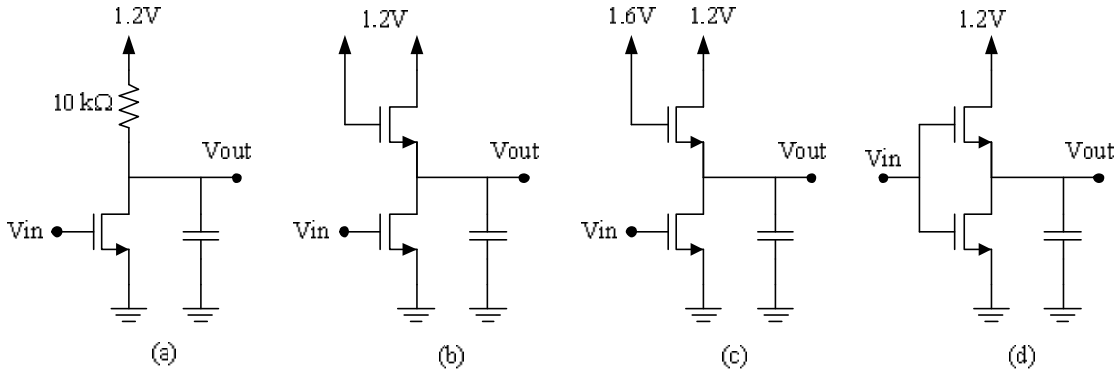

Fig. 6

7. (16%) Design a 5 GHz ring oscillator using CMOS inverters. Assume the specified inverter has the propagation delay of 0.02 ns with the power supply V_{DD} of 1.8 V, the input capacitor of 30 fF and the output capacitor of 50fF.

(a) How many satges of inverter in cascade do you uesd to form this ring oscillator?
(b) Neglect the short-circuit power dissipation, what is average power comsumption of this ring oscillator design in part (a)?