大同大學 96 學年度研究所碩士班入學考試試題

考試科目：電子學　　所別:電機工程研究所　　

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

1. (16%) (a) The Widlar current source shown in Fig. 1 is biased at V^+=5V, V^- = -5V, V_{BE1}=0.7V with resistor R_1=9.3 KΩ and R_E =9.58 KΩ. Calculate I_{REF} and I_O.
   (b) Derive the output resistance (R_O) and calculate it with BJT's V_A=80 V and β=100.

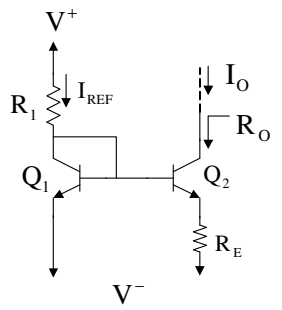

Fig. 1

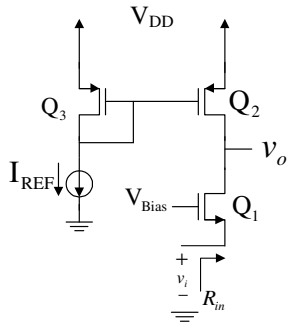

Fig. 2

2. (17%) Refer to Fig. 2, where I_{REF}=100μA and all transistors have W/L=100μm/1.6μm, $\mu_n C_{ox}$=90μA/V^2, $\mu_p C_{ox}$ =30μA/V^2 , $1/\lambda_n$ =V_{An}=12.8V, $1/|\lambda_p|$ =$|V_{Ap}|$=19.2V, and the body effect factor χ=0.15 for Q1. Calculate g_{m1}, g_{mb1}, r_{o1}, r_{o2}, the voltage gain $A_v = \frac{v_o}{v_i}$ and the input resistance R_{in}.
3. (10%) (a) Design an inverting opamp circuit for which the gain is –5V/V and an input resistance of 10kΩ. Draw the circuit.
   (b) If the opamp has an open-loop gain of 600V/V, determine the actual gain of the inverting opamp circuit designed in part (a).
4. (24%) Consider the differential amplifier shown in Fig. 3, where $(W/L)_1=(W/L)_2$=100, $(W/L)_{B1}$=20, $(W/L)_{B2}$=100, and $\mu_n C_{ox}=2.5\times\mu_p C_{ox}$ =100μA/V^2, V_{tn}= -V_{tp}=0.6V, $\lambda_n=\lambda_p$ =0.04 V^{-1}. For DC bias calculations, neglect channel-length modulation effect.
   (a) For I_{bias}=40μA, find the required value of R.
   (b) If the DC voltage at the output is 2V, find the W/L ratio for M3 and M4.
   (c) Determine the low-frequency differential gain (v_{out}/v_d).
   (d) Estimate the –3dB frequency in Hz.
   (e) Find the input common-mode (V_{CM}) range.
5. (25%) (a) Draw the schematic diagram of a CMOS inverter with the substrate connection.
   (b) Draw the input and output voltage transfer characteristic curve with V_{DD} = 3.3 volts, V_{tn} = $|V_{tp}|$ = 1 volt, and define the range in which both transistors are saturated.
   (c) Draw the input voltage V_{in} and the drain current I_{DN} = $|I_{DP}|$ transfer curve.
   (d) Find the $(W/L)_{NMOS}/(W/L)_{PMOS}$ if noise margin NM0 = NM1 is required. Assume $\mu_n C_{ox}$=115 μA/V^2 and $\mu_p C_{ox}$=30 μA/V^2.
   You must label the critical break points in the curves.
6. (8%) The identical NMOS transistors are connected as Fig. 4. Determine the output voltage (V_o) in terms of V_{DD} and V_t, where V_t is the threshold voltage of device. (Neglect the body effect).

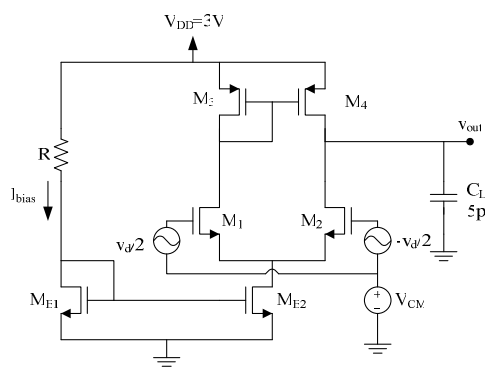

Fig. 3

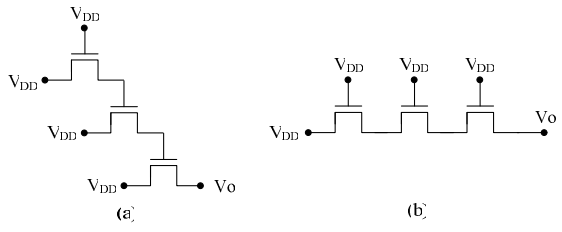

Fig. 4