

# 大同大學 97 學年度研究所碩士班入學考試試題

考試科目：電子學

所別：電機工程研究所

第 1/2 頁

註：本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

1. Consider the circuit shown in Fig. 1.

(a) For both BJTs Q1 and Q2,  $\alpha_1 = \alpha_2 = \alpha$ ,  $I_{S1} = I_{S2} = I_S$ , derive an expression for  $I_{c1}$  and  $I_{c2}$  in terms of  $\alpha$ ,  $I_{EE}$ ,  $V_{id} (=V_{i1} - V_{i2})$  and  $V_T (=kT/q)$  ...etc. (10%)

(b) Show that  $\Delta I_c = I_{c1} - I_{c2} = \alpha I_{EE} \tanh\left(\frac{V_{id}}{2V_T}\right)$ . (6%)

2. (a) Draw the small-signal equivalent circuit for Fig. 2. (include body effect for Q1) (3%)

(b) Derive the voltage gain  $A_v = v_o/v_i$ . (8%)

(c) Let  $W/L = 100\mu\text{m}/2\mu\text{m}$  for all n-MOS,  $\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2$ ,  $I_{REF} = 100\mu\text{A}$ ,  $1/\lambda = 12\text{V}$  and  $g_{mb} = \chi g_m$ ,  $\chi = 0.15$ . Calculate  $A_v = v_o/v_i$ . (6%)

3. Consider the differential amplifier shown in Fig. 3, where  $(W/L)_1 = (W/L)_2 = 100$ ,  $(W/L)_{B1} = 10$ ,

$(W/L)_{B2} = 100$ ,  $\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2$ , and  $V_{tn} = 0.6\text{V}$ . For DC bias calculations, neglect channel-length modulation and body effects.

(a) If the input common-mode voltage  $V_{CM}$  is 1.5V, calculate  $V_p$ . (4%)

(b) If the input common-mode voltage  $V_{CM}$  is 1.5V, determine the output swing range. (4%)

(c) Find the lowest value of  $V_{CM}$  for which  $M_{B2}$  remains in saturation region. (4%)

(d) Determine the low-frequency differential voltage gain  $[(v_{o1} - v_{o2})/v_d]$ . (4%)

(e) Estimate the -3dB frequency in Hz. (4%)

(f) Determine the common-mode gain for  $v_{o1}$  due to the finite drain resistance of  $M_{B2}$ . ( $\lambda = 0.05 \text{ V}^{-1}$ ) (5%)

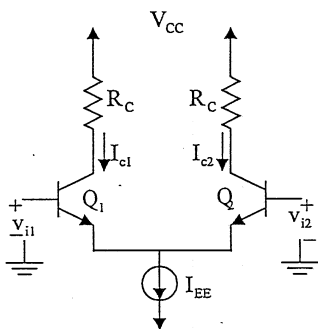


Fig. 1

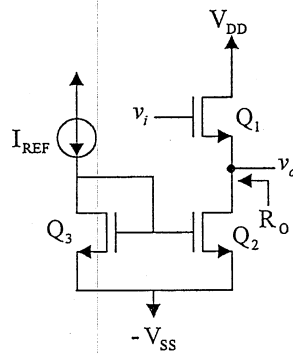


Fig. 2

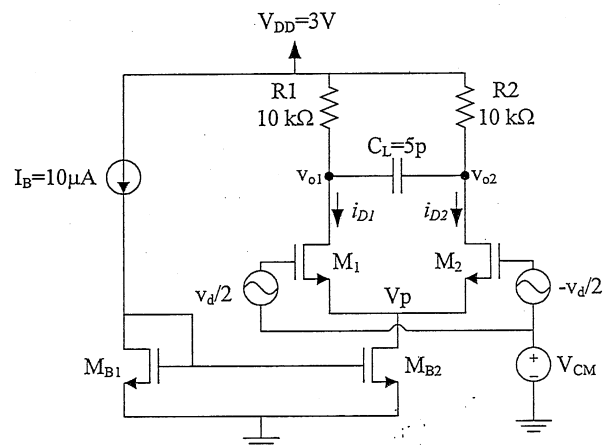


Fig. 3

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考試科目：電子學

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第 2/2 頁

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〈接前頁〉

4. Consider the circuit shown in Fig. 4, where  $(W/L)_1=16$ ,  $(W/L)_2=2.5$ ,  $\mu_n C_{ox}=2.5 \times \mu_p C_{ox}=100 \mu A/V^2$  and  $V_{tn}=-V_{tp}=0.6V$ . Neglect channel-length modulation effect.
- (a) Calculate the small-signal voltage gain of the circuit. (4%)
- (b) Calculate the pole associate with node X. Neglect the gate capacitance of  $M_1$ . (4%)

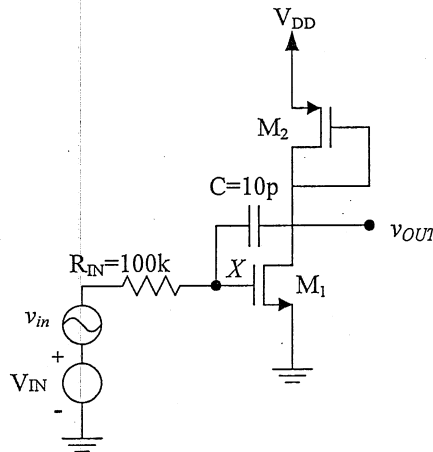


Fig. 4

5. A simplified TTL inverter is shown in Fig. 5. Assume  $\beta_F = 50$  and  $\beta_R = 0.2$ .
- (a) Calculate the power supply currents for  $V_{in} = 0.1 V$  and  $V_{in} = 4 V$ . (10%)
- (b) State the mode of operation for each transistor in both cases. (6%)
6. Find all the voltages at all the nodes for the pass transistor circuit of Fig. 6 neglecting the body effect. Assume  $V_{tn} = |V_{tp}| = 0.4 V$ . (18%)

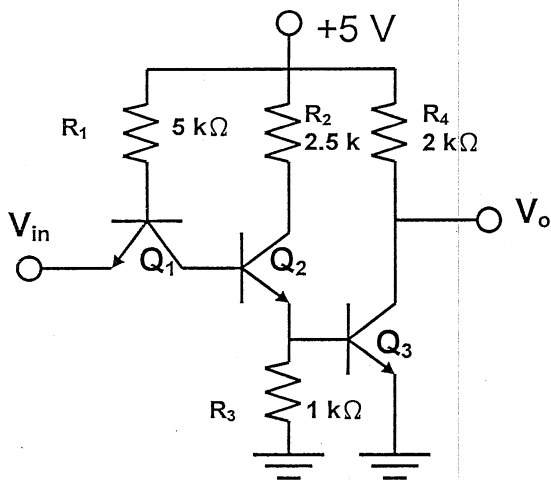


Fig. 5

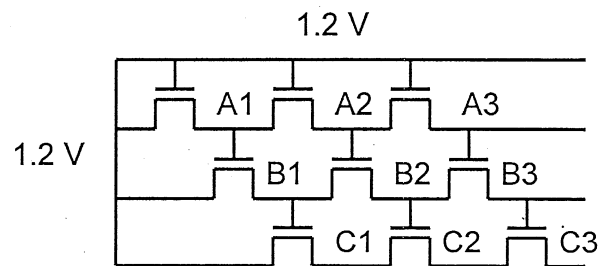


Fig. 6