大同大學 98 學年度研究所碩士班入學考試試題

考試科目：電子學　　所別：電機工程研究所　　

註：本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

1. The circuit as shown in Fig.1, $R_1 = 5\,\mathrm{K\Omega}$, $R_2 = 10\,\mathrm{K\Omega}$, the diode cut-in voltage $V_{D0} = 0.7\mathrm{V}$, draw the V_O vs V_I plot, calculate and indicate the voltages at the breakpoints. (13%)

2. Three-stage amplifier as shown in Fig.2, neglect other capacitances and assuming identical MOS transistors with λ=0.
   (a) In terms of transconductance g_m, R_D and C, derive the transfer function $A(s) = \frac{V_o}{V_i}$. (7%)
   (b) $A(j\omega) = A(s)\big|_{S=j\omega} = |A(j\omega)|e^{j\phi}$, write an expression for $|A(j\omega)|$, and draw the Bode plot $|A(j\omega)|_{dB}$ vs ω (log scale). (6%)
   (c) If we apply negative feedback with feedback factor β=1 around the amplifier, determine the condition for the amplifier to be stable. (6%)

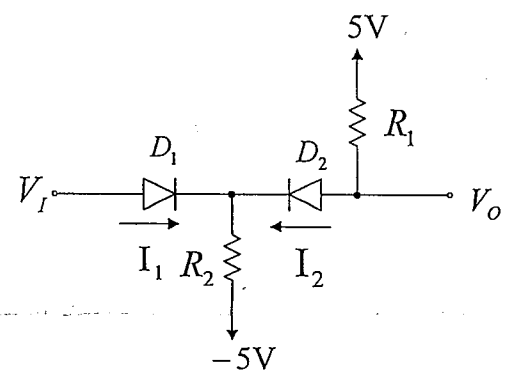

Fig.1

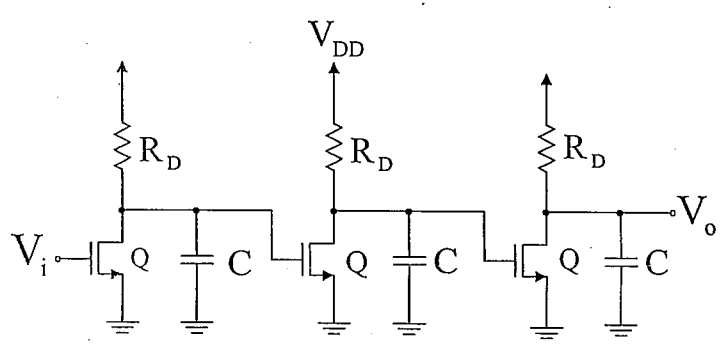

Fig.2

3. For the MOS current-steering circuit shown in Fig. 3, I_{REF}=100 μA, $\mu_n C_{ox}$ = 160 μA/V², $\mu_p C_{ox}$ = 64 μA/V², V_{tn}=0.5V, V_{tp}=-0.6V, $(W/L)_1$=20, $(W/L)_2$=30, $(W/L)_{3,4}$=75 and $(W/L)_{5,6}$=150.
   (a) Neglecting channel-length modulation and body effects, determine I_1, I_2 and V_{G3}. (8%)
   (b) Determine the maximum allowable voltage at the output. (4%)
   (c) Find the output resistance R_o. (λ= 0.05 V^{-1}) (5%)

4. Consider the differential pair shown in Fig.4, where $\mu_n C_{ox}$ = 160 μA/V², V_{tn}=0.5V and $(W/L)_{1,2}$=20.
   (a) Find the minimum required voltage for v_{IN} such that i_{D1}= I_B and i_{D2}=0. (4%)
   (b) Draw i_{D1} and i_{D2} with respect to v_{IN} for Fig.4. Show the critical voltage and current values. (5%)

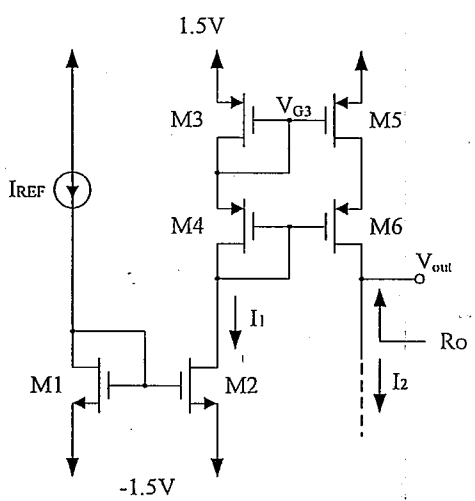

Fig.3

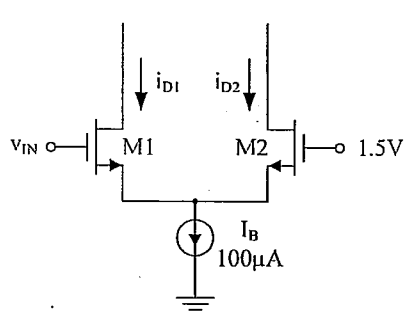

Fig.4

<背面繼續>

大同大學 98 學年度研究所碩士班入學考試試題

考試科目：電子學　　所別：電機工程研究所　　

註：本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

<接前頁>

5. Consider the common-source amplifier shown in Fig.5, where V_{DD}=3V, $\mu_n C_{ox}$ = 160 μA/V^2, $\mu_p C_{ox}$ = 64 μA/V^2, V_{tn}=0.5V, V_{tp}=-0.6V, $(W/L)_1$=20, $(W/L)_{2\text{-}3}$=50 and I_B=100 μA. The DC voltage V_{IN} is chosen such that all transistors are biased in the saturation region.

   (a) Estimate the low-frequency voltage gain for the amplifier. ($\lambda_n = \lambda_p$ =0.05 V^{-1}) (5%)

   (b) Estimate the -3dB bandwidths for the amplifier with R_S =1MΩ and C_L=5pF. Assume C_L is the total capacitance at the output node. (C_{gs1}=0.2pF and C_{gd1}=0.02pF) (5%)

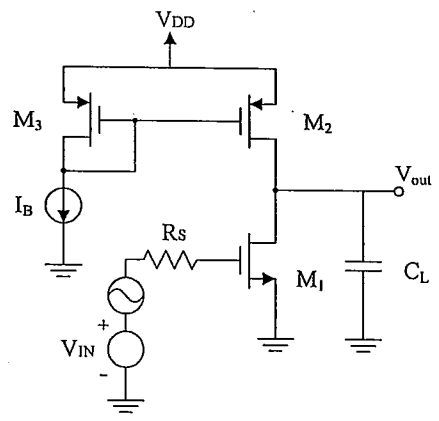

Fig.5

6. The circuits of Fig.6 show different implementations of an inverter whose output is connected to a capacitors. (20%)

   (a) Which one of the circuits consumes static power when the input is high?

   (b) Which one of the circuits consumes static power when the input is low?

   (c) V_{OH} of which circuit(s) is 1.2 V?

   (d) V_{OL} of which circuit(s) is 0 V?

   (e) The proper functionality of which circuit(s) depends on the size of the devices?

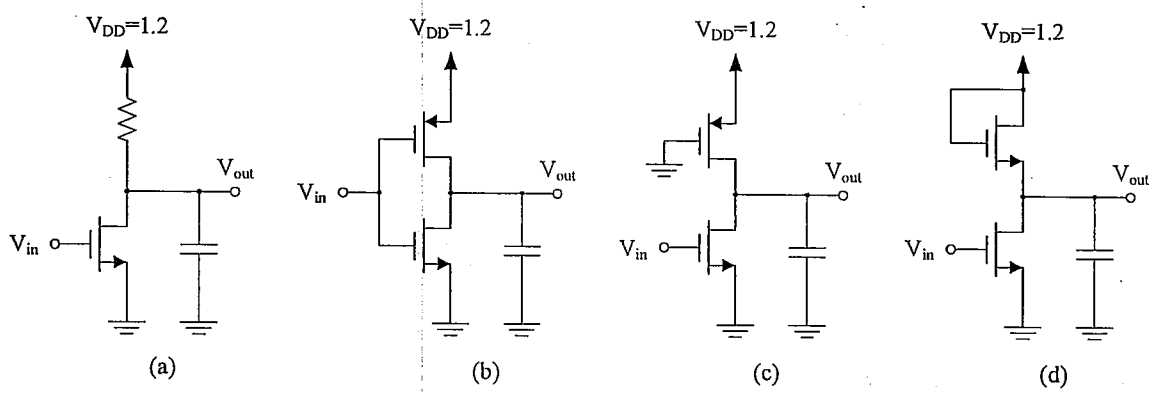

Fig.6

7. (a) Design a static CMOS gate that performs the Boolean function F = (A⊕B)C + BC. You can use inverters to generate any complementary inputs needed. Sizing is not required here. (6 %)

   (b) Find the logic function for the circuit in Fig.7. (6 %)

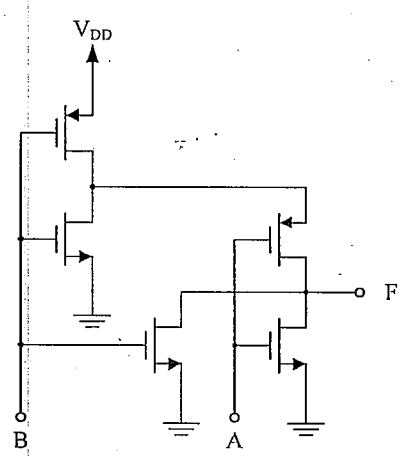

Fig.7