大同大學 99 學年度研究所碩士班入學考試試題

考試科目:電子學　　所別:電機工程研究所　　

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器。

1. (10%) Assume the diodes in the circuit of Fig. 1 to be ideal.
   (a) Derive the relationship of v_O and v_I.
   (b) For $-10V \le v_I \le 10V$, draw the v_O vs v_I plot and indicate the voltages at the breakpoints.

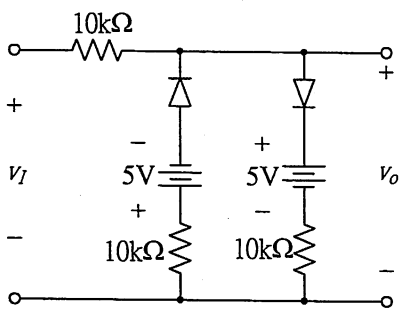

Fig. 1

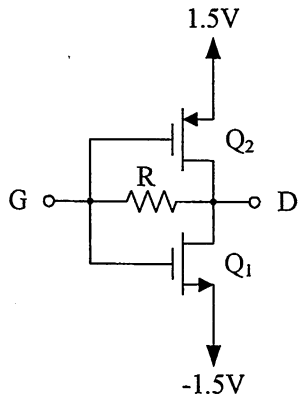

Fig. 2

2. (24%) The MOSFETs in the circuit of Fig. 2 are matched, having $\mu_n C_{ox}(W/L)_n = \mu_p C_{ox}(W/L)_p = 1mA/V^2$, $|V_{tn}| = |V_{tp}| = 0.5V$, and the resistance R=1MΩ.
   (a) For G and D open, calculate the dc voltage at G (V_G) and dc drain current $I_{D1}(Q_1)$ and $I_{D2}(Q_2)$.
   (b) For finite r_o ($\lambda_n = |\lambda_p| = 0.05\ V^{-1}$), draw the small-signal equivalent circuit, calculate the voltage gain (v_d / v_g) from G to D and find the input resistance (R_{in}) at G.

3. (10%) Find V_1, V_2 and I_1~I_3 in the circuit shown in Fig. 3. Assume $|V_{BE}|=0.7V$ and $\beta=\infty$.

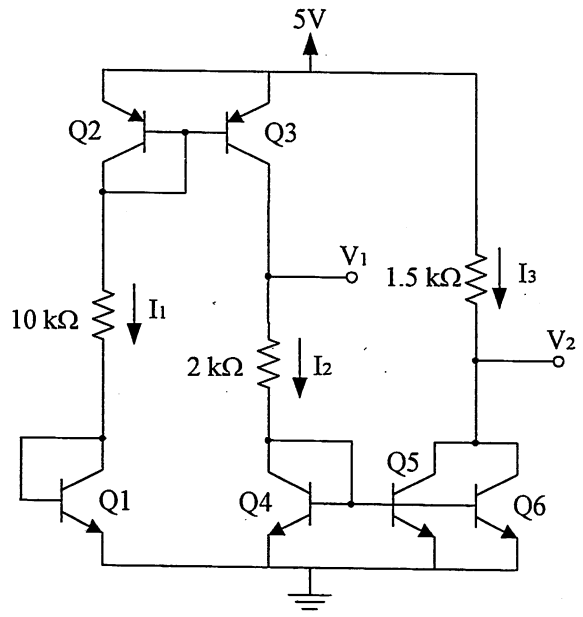

Fig. 3

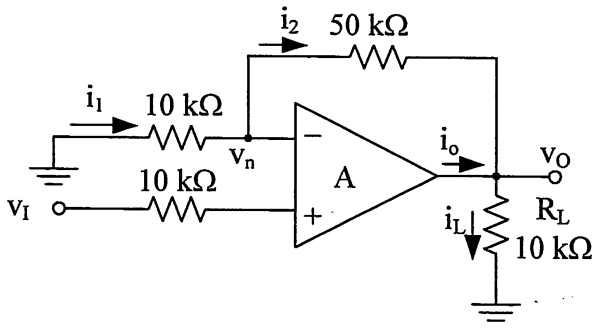

Fig. 4

4. (14%) Consider the circuit shown in Fig. 4.
   (a) Identify the feedback topology, and find the feedback factor β.
   (b) If the opamp is ideal, find the closed-loop gain v_O/v_I.
   (c) If the opamp gain is A=300, find the closed-loop gain v_O/v_I.
   (d) The ideal opamp is specified to have output current limits of ±20mA. If the circuit is fed with a low-frequency sine-wave signal of peak voltage 0.5V, what is the lowest value of R_L for which an undistored sine-wave output is obtained?

〈背面繼續〉

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5. (12%) Consider the common-source amplifier shown in Fig.5, where V_{DD}=3.3V, $\mu_n C_{ox}$ = 200 μA/V^2, $\mu_p C_{ox}$ = 80 μA/V^2, V_{tn}=0.5V, V_{tp}=-0.6V, $(W/L)_1$=20, $(W/L)_{2,3}$=50 and I_B=125 μA.
   (a) Calculate the required input DC voltage V_{IN} such that all transistors are biased in the saturation region.
   (b) Estimate the low-frequency voltage gain for the amplifier. ($\lambda_n = |\lambda_p| = 0.05\ V^{-1}$)
   (c) Estimate the -3dB bandwidths for the amplifier with C_L=5pF. Assume C_L is the total capacitance at the output node.

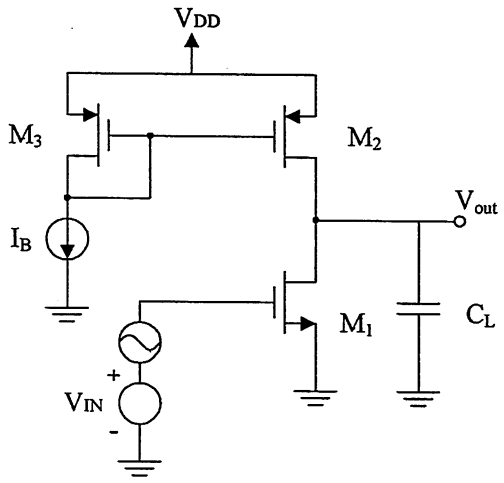

Fig. 5

6. (18%)
   (a) Draw the schematic diagram of a CMOS inverter with the substrate connection.
   (b) Find the input range which causes a direct-path current, i. e. both transistors are conducted simultaneously, if the inverter has the power supply V_{DD} = 3.3 Volts and the device threshold voltage is $V_{tn} = |V_{tp}|$ = 0.7 volts.
   (c) If a CMOS inverter has the load capacitance C_L, then the direct-path current is function of the rise time, falling time and C_L. How does it affect the direct-path current when the rise time and C_L are increased repectively?

7. (12%) Please write down the Boolean functions of the CMOS circuits shown in Fig. 6 and identify these logic functions (AND, OR, XOR, MUX etc.) performed.

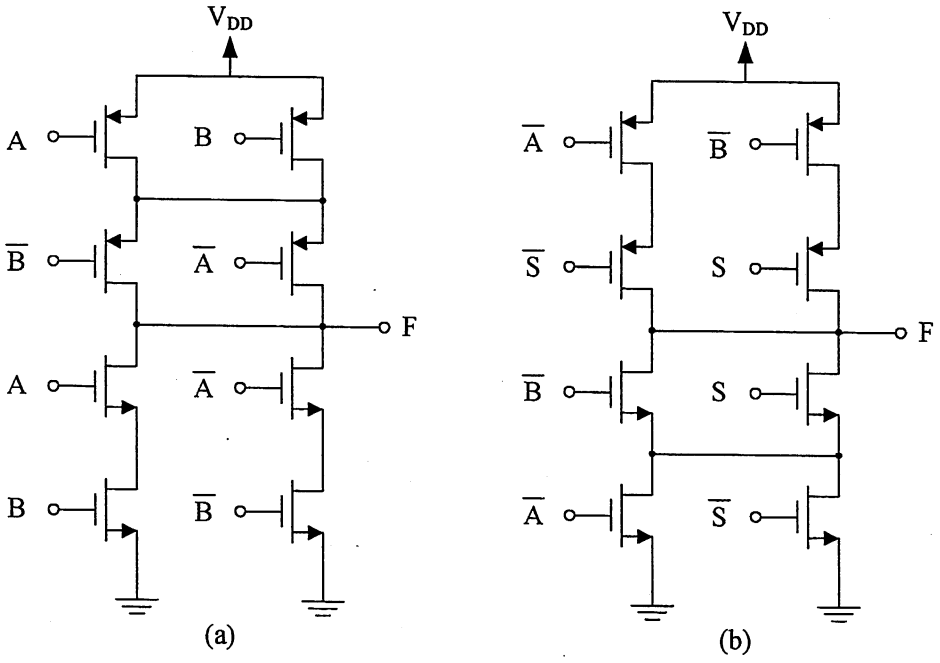

Fig. 6