

大同大學 九十 學年度研究所碩士班入學考試試題

考試科目：計算機組織

所別：資訊工程研究所

第 $\frac{1}{3}$ 頁

註：本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 不可以使用計算器。

Prob. 1. List all the necessary considerations for the design of the CPU instruction set for modern digital computer systems. (10%)

Prob. 2. Suppose we could improve the speed of the CPU in our machine by a factor of five (without affecting I/O performance) for five times the cost. Also assume that the CPU is used 50% of the time, and rest of the time the CPU is waiting for I/O. If the CPU is one-third of the total cost of the computer, is increasing the CPU speed by a factor of five a good investment from a cost/performance viewpoint? (10%)

Prob. 3. Consider the execution of 1000 instructions using a 6-segment pipeline. (10%)

1. What is the average number of instructions executed per instruction cycle when $C=0.2$?
2. What must be the value of C so execution of at least 4 instructions per instruction cycle is always allowed?

Note: C is the probability for an instruction to be a branch instruction, and each branch instruction requires 4 additional clock cycles.

Prob. 4. In a memory hierarchy that includes a TLB and a cache, a memory reference can encounter three different types of misses: a cache miss, a TLB miss, and a page fault. Consider all the combinations of these three events with one or more occurring (seven possibilities). For each possibility, state whether this event can actually occur and under what circumstances. (10%)

Prob. 5. Describe the functions of the following devices or technologies. (18%)

1. addressing mode
2. memory-mapped I/O
3. Register window
4. Microprogramming
5. delayed branch
6. interleaved memory

Prob. 6. You purchased a computer with the following features:

- 90% of all memory accesses are found in the cache.
- Each cache block is four words, and the whole block is read on any miss.
- The processor sends references to its cache at the rate of 10^9 words per second.
- 30% of those references are writes.
- Assume that memory system can support 10^9 words per second, reads or writes.
- The bus reads or writes a single word at a time (the memory system cannot read or write two words at once).
- Assume at any one time, 30% of the blocks in the cache have been modified.
- The cache uses write allocate on a write miss.

You are considering adding a peripheral to the system, and you want to know how much of the memory system bandwidth is already used. Calculate the percentage of memory system bandwidth used on the average in the two cases below. Be sure to state your assumptions. (14%)

1. The cache is write through.
2. The cache is write back.

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Prob. 7.(28%) Circle all correct answers in each of the following questions. Some of the questions may have more than one correct answer. The penalty of selecting wrong answer in any question is to receive a zero credit for that question.

1. For implementing a high performance I/O bus, we should use
(a) synchronous clocking (b) asynchronous clocking (c) multiple bus master
(d) separate address and data line (e) single master
2. Page fault interrupt may occur in which cycle(s)?
(a) instruction fetch (b) decode and register fetch (c) execution (d) memory (e) write back
3. The maximum speedup of using a pipeline processor with k stages for the execution of a vector instruction of length n is equal to
(a) n (b) k (c) n/k (d) n+k (e) n+k-1
4. In a paged memory system, the following statement (or statements) is (or are) more often true than false for a random program mix.
(a) The locality of references leads to the use of limited working sets.
(b) The least recently used (LRU) replacement algorithm results in less page faults than the FIFO algorithm.
(c) The random replacement policy performs better than the LRU algorithm.
(d) The hit ratio has nothing to do with page sizes.
5. In a cache memory system, a conflict misses will occur, if the block placement strategy is
(a) set associative mapping. (b) fully associative mapping. (c) direct mapping. (d) none of the above.
6. A tightly coupled MIMD multiprocessor system should have
(a) shared main memory which is accessible by all processors.
(b) only private memory local to each processor.
(c) multiple operating systems run independently on different processors.
(d) an integrated operating system for entire system.
7. The processing units in a SIMD computer are followed to operate
(a) asynchronously to execute different instructions at the same time.
(b) synchronously to execute different instructions at the same time.
(c) synchronously to execute the same instruction at the same time.
(d) in none of the above modes.
8. In a paged memory system, the following statement (or statements) is (or are) more often true than false for a random program mix.
(a) The locality of references leads to the use of limited working sets.
(b) The least recently used (LRU) replacement algorithm results in less page faults than the FIFO algorithm.
(c) The random replacement policy performs better than the LRU algorithm.
(d) The hit ratio has nothing to do with page sizes.
9. As far as the general application of computer is concerned,
(a) SIMD computers are more flexible than MIMD computers.
(b) the performance of a pipelined processor is independent of the vector length.
(c) SIMD and MIMD computers are both for general purpose applications.
(d) none of the above is true.

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10. In a lookahead processor with both input (domain) and output (range) buffering, the following condition(s) can be removed in determining the dependency between two instructions, I followed by J in a program.
- (a) $D(J) \cap R(I) \neq 0$
 - (b) $D(I) \cap R(J) \neq 0$
 - (c) $R(I) \cap R(J) \neq 0$
 - (d) none of the above

11. Consider the execution of the following program in either scalar mode, or vector mode, or multitasked vector mode.

```
DO 10 I= 1, N
  A(I) = B(I) + S * C(I)
10 CONTINUE
```

- (a) Under no circumstances, the scalar mode should be chosen.
- (b) When N is large and the overhead of multitasking is very high, vector mode should be chosen.
- (c) When N is very large and the multitasking overhead is low, then multitasked vector mode is appropriate.
- (d) Multitasking should always be chosen at the expense of vectorization.

(12-14) Given the following system statistics:

```
system up 8 hours
system down 2 hour
system up 10 hours
system down 2 hours
system up 6 hours
system down 2 hour
```

Handwritten calculations:

$$\frac{10}{10+2} = 0.833$$
$$12 \overline{) 100} \\ \underline{96} \\ 40$$

respond to the following 3 questions.

- 12. The MTTF is (a) 8 hours (b) 6 hours (c) 4 hours (d) 10 hours (e) 18 hours (f) none of the above
- 13. The MTTR is (a) $\frac{3}{5}$ hour (b) $\frac{5}{3}$ hour (c) $\frac{4}{3}$ hours (d) 2 hours (e) 4 hours (f) none of the above
- 14. The percentage of system availability is (a) 100% (b) 90% (c) 80% (d) 82% (e) none of the above