大同大學 九十一 學年度研究所碩士班入學考試試題

考試科目:計算機組織　　所別:資訊工程研究所　　

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 不可以使用計算器。

1. A new microprocessor is being designed with a conventional architecture employing single-address instructions and 8-bit words. Due to physical size constrains, only eight distinct 3-bit opcodes are allowed. The use of modifiers or the address field to extend the opcodes is forbidden.

   (a) What eight instructions would you implement? Specify the operations performed by each instruction as well as the location of its operands. (8%)
   (b) Demonstrate that your instruction set is functionally complete in some reasonable sense; if it is not, describe an operation that can not be programmed using your instruction set. (8%)

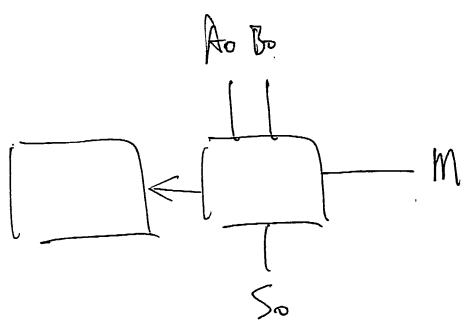
2. (a) Draw a diagram to show a single-bus orgnization of the data path inside the CPU. (8%)
   (b) According to the structure in (a), write a control sequence for execution of the instruction "Add contents of a memory location addressed in absolute mode to a register, say R1." (8%)
   (c) The CPU is driven by a continuously running clock, such that each control step is 100*ns* in duration. How long will the CPU have to wait for memory function complete, assuming that a memory read operation takes 0.4 μs to complete? What percentage of time is the CPU idle during execution of this instruction? (8%)

3. Describe the properties of the following memory devices: (16%)
   (a) DRO memory (b) interleaved memory (c) flash memory (d) SDRAM

4. A computer consists of a CPU and an IO device D connected to main memory M via a one-word shared bus. The CPU can execute a maximum of 10^5 instructions per second. An average instruction requires 5 machine cycles, three of which use the memory bus. A memory read or write operation uses one machine cycle. When not executing IO instructions, the CPU operates at 95% of its maximum speed. The IO device D is only used to transfer large blocks of data to and from M.

   (a) If programmed IO is used, and each one-word IO transfer requires the CPU to execute 2 instructions, estimate the maximum IO data transfer rate r_{max} possible through D. (8%)
   (b) Estimate r_{max} if DMA transfer is used. (8%)

5. A nonpipeline system takes 50*ns* to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10*ns*. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? (8%)

6. Design a fast 16-bit adder by using the 4-bit carry-lookahead adder as a building block. Eastimate the worst-case add-time of your design, and compare it with a 16-bit Ripple-carry Adder. Assume that the gate dealy is *d* time units. (12%)

7. Our favorite program runs in 12 seconds on computer A, which has a 400MHz clock. We are trying to help a computer designer build a machine B that will run this program in 6 seconds. The designer has determined that a substantial increase in clock rate is possible, but this increase will affect the rest of the CPU design, causing machine B to require 1.2 times as many clock cycles as machine A for this program. What clock rate should we tell the designer to target? (8%)