大同大學 九十二 學年度研究所碩士班入學考試試題

考試科目:計算機組織　　所別:資訊工程研究所　　

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 不可以使用計算器。

1. (15%)
Explain the following terms as clear as you can: (1). *Throughput*; (2). *Stack frame*; (3). *Delayed branch*; (4). *Data hazards*; (5). *Aliasing*.

2. (10%)
   (a) What is *Amdahl's Law*? (5%)
   (b) Suppose we could improve the speed of the CPU in our machine by a factor of 5 (without affecting I/O performance) for 7 times of the cost. Also assume the CPU is used 75% of the time, the rest of the time the CPU is waiting for I/O. If the CPU is 40% of the total cost of the computer, is increasing the CPU speed by a factor of 5 a good investment from cost/performance viewpoint? Justify your answer.

3. (15%)
The performance of a 100 MHz microprocessor X is measured by executing 10,000,000 instructions of benchmark code, which is found to take 0.25s.
   (a) What are the value of CPI for this performance experiment?
   (b) What are the value of MIPS for this performance experiment?
   (c) Is X likely to be superscalar? Why ?

4. (20%)
Consider a 32-bit RISC-style processor p whose only addressing modes for register to register instructions are immediate and direct and whose only addressing mode for load/store instructions is register indirect with offset. Assume also that the CPU has 32 general-purpose registers $R_0 \sim R_{31}$ that can serve either as data or address registers. A single 32-bit instruction fomat contains four fields: an opcode, two register fields, and a 16-bit iemmediate field.
   (a) What is the maximum number of opcode types? (5%)
   (b) Using an *adhoc* but typical assembly language notation with clear comments, describe how a single instruction of p might perform each of the following three operations: load a word from memory; store a byte into memory; double the number word stored in a register (there is no multiply opcode). (6%)
   (c) Describe how one or more instructions of p might perfom each of the following three operations, assuming that p has no explicit *clear, swap, or push* opcodes: clear a register; swap the contents of two registers; push a word into a stack. Use as few instructions as you can. (9%)

5. (20%)
   (a) Use IEEE 754 folating point standard to answer the following questions.
      i. Do $X - Y$ with $X = 1.00\cdots00 \times 2^1$ and $Y = 1.11\cdots11 \times 2^0$ without a *guide bit*.
      ii. Do $X - Y$ with $X = 1.00\cdots00 \times 2^1$ and $Y = 1.11\cdots11 \times 2^0$ with a *guide bit*.
   (b) Using hexadecimal system to do the above problems. (5%)
   (c) What are the 4 modes of rounding used in IEEE 754 folating point standard? (5%)

6. (10%)
A certain processor has a microinstruction format containing 10 separate control fields $C_0 \sim C_9$. Each C_i can activate any one of n_i distinct control lines, where n_i is specified as follows:

$i =$	0	1	2	3	4	5	6	7	8	9
$n_i =$	4	4	3	11	9	16	7	1	8	22

   (a) What is the minimum number of control bits needed to represent the 10 fields?
   (b) What is the maximum number of control bits needed if a purely horizontal format is used for all the control information?

7. (10%)
Suppose we have a processor with a base CPI of 1.0, assuming all data references hit in the primary cache, and a clock rate of 500 MHz. Assume a main memory access time of 200 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 5%. How much faster will the machine be if we add a secondary cache that has a 20 ns access time and is large enough to reduce the miss rate to main memory to 2%?