大同大學 九十三 學年度研究所碩士班入學考試試題

考試科目:計算機組織　　所別:資訊工程研究所　　

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 不可以使用計算器。

Prob. 1. Consider the following possibilities for saving the return address of a subroutine:

(a) In a processor register

(b) In a memory location associated with the call, so that a different location is used when the subroutine is called from different places.

(c) On a stack

Which of these possibilities supports subroutine nesting and which supports subroutine recursion (that is, a subroutine that calls itself)? Explain your answer. (10%)

Prob. 2.

(1). Describe the reason why the biased exponent is usually used in the floating-point representation? (6%)

(2). Follow the IEEE 754 floating-point standard to represent a decimal number -6.5625 in single-precision format. (6%)

(3). What problems do you encounter when trying to convert the following decimal numbers into IEEE standard single-precision floating-point format? (8%)

(i) $7.1239 * 10^{51}$

(ii) $-1.4325 * 10^{-27}$

Prob. 3. (20%) There are 4 architecture styles: Accumulator, Memory-Memory, Load-Store, and Stack. Write the four code sequences for the C code $a = b + c - d$ using assembly language with minimum instruction counts in each architectural style. For each code sequence, calculate the instruction bytes fetched and memory-data bytes transferred (read or write). Assume:

- The opcode is always 1 byte.
- All memory addresses are 2 bytes.
- All data operands are 2 bytes.
- All instructions are in an integral number of bytes in length.
- The variables a, b, c, and d are initially in memory.
- For load-store architecture, there are 16 general purpose registers.

Prob. 4. What are the hazards in an instruction pipeline? Describe the possible solutions to minimize the hazard stalls for each hazard.(15%)

Prob. 5. A computer system has a main memory consisting of 1M 16-bit words. It also has a 4K-word cache organized in the set-associative manner, with four blocks per set and 64 words per block.

(1) Calculate the number of bits in each of the Tag, Index (Set), and Word (offset in the block) fields of the main memory address. (5%)

(2) Assume that the cache is initially empty. Suppose that the CPU fetches 4352 words from locations 0,1, 2,…,4351 (in that order). It then repeats this fetch sequence nine more times. If the cache is 10 times faster than the main memory, estimate the improvement factor resulting from the use of the cache. Assume that the LRU algorithm is used for block replacement.(10%)

Prob. 6. Describe the functions of the following devices or technologies. (20%)

(1). memory-mapped I/O

(2). interleaved memory

(3). DMA

(4). TLB

(5) Microprogramming