大同大學 九十四 學年度研究所碩士班入學考試試題

考試科目:計算機組織　　所別:資訊工程研究所　　

註:本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 不可以使用計算器。

1. Assume that multiply instructions takes 12 cycles and account for 15% of the instructions in a typical program, and the other 85% of the instructions require an average of 4 cycles for each instruction. What percentage of time does the CPU spend doing multiplication? (6%)

2. You are considering such a project for translating VAX code to MIPS code. The question of interest is what will be the instruction count increase arising from translating the VAX memory operands and addressing modes. Ignoring all other issues, find the average number of MIPS instructions per VAX instruction using the following data. Assume that all VAX displacements fit in the MIPS displacement field. (10%)

   For VAX program:
   19% immediate operand
   50% register operand
   31% memory operand

   Use of VAX memory addrsssing modes:
   22% register deferred
   63% displacement
   12% indexed
   3% displacement deferred

   Hint:
   (i) Ignoring the fact that we overestimate the number of translated MIPS instructions needed for VAX load and store instructions.
   (ii) Register deferred and displacement addressing modes can be described by MIPS addressing mode.
   (iii) Indexed and displacement deferred require 2 MIPS instructions to build those addressing modes.

3. Comparing and contrasting ripple-carry adder and carry-lookahead adder in terms of speed, hardware complexity and the handling of signed binary numbers. (Note that addition of a negative number corresponds to subtraction of a positive number.) (12%)

4. A computer has a two-level virtual memory system. The main memory M1 and the secondary memory M2 have average access times of 10^{-6} and 10^{-3} s, respectively. It is found by measurement that the average access time for the memory hierachy is 10^{-4} s, which is considered unacceptably high. Describe two ways in which this memory access time could be reduced from 10^{-4} to 10^{-5} s and discuss the hardware and software costs involved. (12%)

5. Suppose a computer's address size is k bits (using byte addressing), the cache size is S bytes, the block size is B bytes, and the cache is A-way set-associative. Assume that B is a power of two, so $B=2^b$. Figure out what the following quantities are in terms of S, B, A, b, and k:
   (a) the number of sets in the cache, (4%)
   (b) the number of index bits in the address, (4%)
   (c) the the number of bits needs to implement the cache. (4%)

6. A pipeline P is found to provide a speedup of 6.16 when operating at 100 MHz and an efficiency of 88 percent.
   (a) How many stages does P have? (5%)
   (b) What are P's MIPS and CPI performance levels? (5%)

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7. Suppose we have a system with the following characteristics:
   (i) A memory and bus system aupporting block access of 4 to 16 32-bit words.
   (ii) A 64-bit synchronous bus clocked at 200 MHz, with each 64-bit transfer taking 1 clock cycle, and 1 clock cycle required to send an address to memory.
   (iii) Two clock cycles needed between each bus operation. (Assume the bus is idle before an access.)
   (iv) A memory access time for the first 4 words of 200 ns; each additional set of 4 words can be read in 20 ns. Assume that a bus transfer of the most recenctly read data and a read of the next 4 words can be overlapped.
   (v) The first 4 words are written 200 ns after the address is available, and each new write takes 20 ns. Assume a bus transfer of the most recent data to write, and a write of the previous 4 words can be overlapped.

   Find the sustained bandwidth and the latency for
   (a) a read of 256 words for transfers that use 16-word blocks. (6%)
   (b) a write of 256 words for transfers that use 16-word blocks. (6%)
   (c) a write of 256 words for transfers that use 16-word blocks, if the 64-bit bus is separated as 32-bit address and data lines. (6%)

8. State whether the following techniques or components are associated primarily with a software- or hardware-based approach to exploiting ILP (Instruction-Level Parallelism). In some cases, the answer may be both. (20%)

   (a) Branch prediction (b) Multiple issue (c) Superscalar (d) Dynamic scheduling
   (e) Out-of-order execution (f) Speculation (g) Reorder buffer (h) Register renaming
   (i) VLIW(Very Long Instruction Word) (j) EPIC(Explicitly Parallel Instruction Computer)