

大同大學 95 學年度研究所碩士班入學考試試題

考試科目: 計算機組織

所別: 資訊工程研究所

第1/2頁

註: 本次考試 不可以 參考自己的書籍及筆記; 不可以 使用字典; 不可以 使用計算器。

1. Briefly answer the following questions: (20%)

- (a) What is the difference between standard I/O and memory-mapped I/O?
- (b) What is the interleaved memory?
- (c) What is meant by DMA in I/O system?
- (d) What is the function of a Translation Lookaside buffer?
- (e) What is the difference between standard I/O and memory-mapped I/O?

2. Consider the 64-bit IEEE 754 floating-point number format. Determine the largest positive number, the smallest nonzero positive number, and the negative number with the largest magnitude that can be represented in this format. Assume the three numbers are to be normalized, and give your answers in the form of 16-digit hexadecimal strings. (12%)

3. Match the addressing modes shown in column 1 with the applications listed in column 2. (16%)

- | | |
|-----------------------|--|
| (a) Register | 1. For stepping through arrays within a loop |
| (b) Immediate | 2. Useful for accessing static data |
| (c) Displacement | 3. Used to index arrays |
| (d) Register deferred | 4. Value is in a register |
| (e) Indexed | 5. Accessing local variables |
| (f) Direct/Absolute | 6. Useful in array addressing |
| (g) Autoincrement | 7. Accessing using a pointer or a computed address |
| (h) Scaled (Index) | 8. For constants |

4. Given the following terms associated with a linear pipelined processor:

k = the number of pipeline stage,
 n = the number of operations to be performed,
 τ = the pipeline clock period. Assume one result per clock period.

Derive the following performance expressions in terms of k , n , and τ . (16%)

- (a) S_k : the speedup of using the pipeline over an equivalent function but non-pipelined processor.
- (b) η : the efficiency of the pipeline.
- (c) W : the throughput of the pipeline.
- (d) What is the relationship between the throughput W and the efficiency η ?

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第2/2頁

註:本次考試 不可以參考自己的書籍及筆記; 不可以使用字典; 不可以使用計算器。

5. A typical computer system has 32M main memory and 4K fully associated cache memory. The cache block size is 8 words. The access time for the main memory is 10 times that of the cache memory.

- (a) How many hardware comparators are needed? (3%)
- (b) What is the size of the tag field? (3%)
- (c) If a direct mapping scheme were used instead, what would be the size of the tag field? (3%)
- (d) Suppose the access efficiency is defined as the ratio of the average access time with a cache to the average access time without cache, determine the access efficiency assuming a cache hit ratio H of 0.9. If the cache access time is 200ns, what hit ratio would be required to achieve an average access time equal to 500ns? (5%)

6. The CPU of a computer contains 8 registers R0 through R7. The register R7 is a read-only register and it always contains a zero. The instruction set of this machine includes the following instructions:

ADD Ri, X, Rj ; $R_j \leftarrow (R_i) + \text{Memory}(X)$, where $i = 0, 1, \dots, 7$ but $j = 0, 1, \dots, 6$.
ADD Ri, Rj, X ; $\text{Memory}(X) \leftarrow (R_i) + (R_j)$, where $i, j = 0, 1, 2, \dots, 6, 7$

Note: The instruction set does not have any explicit memory to register or register to memory load and store instruction.

- (1) Write a program segment to move the content of memory location 1000 to memory location 2000. (5%)
- (2) Write another program segment that will add the contents of memory locations 2400 and 2500 and save the sum in memory location 2600. (5%)

7. Suppose the branch frequencies (as percentages of all instructions) are as follows:

Conditional branches	20%
Jumps and calls	5%
Conditional branches	60% are taken

We are examining a four-deep pipeline where the branch is resolved at the end of the second cycle for unconditional branches, and at the end of the third cycle for conditional branches. Assuming that only the first pipe stage can always be done independent of whether the branch goes and ignoring other pipeline stalls, how much faster would the machine be without any branch hazards? (12%)