大同大學 96 學年度研究所碩士班入學考試試題

考試科目：計算機組織　　所別：資訊工程研究所　　

註：本次考試 不可以參考自己的書籍及筆記； 不可以使用字典； 可以使用計算器

1. (10%)
The value represented by the hexadecimal number 1234 5678 ABCD EF09 is to be stored in an aligned 64-bit double word. Assume the word address is 0000 0000_{16}

   (a) Show the value stored at each byte using Big Endian order.

   (b) Show the value stored at each byte using Little Endian order.

2. (15%)

   (a) What is overflow means?

   (b) Use two 8-bit numbers as an example to show the occurring of overflow.

   (c) How to detect overflow in hardware?

3. (10%)
Consider program P, which runs on a 1 GHz machine M in 10 seconds. An optimization is made to P, replacing all instances of multiplying a value by 4 (mult X, X, 4) with two instructions that set x to x + x twice (add X,X; add X,X). Call this new optimized program P'. The CPI of a multiply instruction is 4, and the CPI of an add is 1. After recompiling, the program now runs in 9 seconds on machine M. How many multiplies were replaced by the new compiler?

4. (15%)

   (a) Show the IEEE 754 binary representation of the number -0.75_{10} in a single precision form. Using hexadecimal form in your answer.

   (b) What decimal number is represented by this single precision floating point number: C0 A0 00 00_{16} ?

   (c) Do $(1.010 \times 2^3) \times (1.010 \times 2^2)$ by using binary floating point format with 3 digits after binary point precision. Show the g, r and s bits during each operation step.

5. (20%)
Suppose there are two machines A and B with same native CPI (cycles per instruction, C). Following table is the associated cache system for machines A and B.

	cache size	miss rate	clock cycle time
Machine A	32KB	2%	$2ns$
Machine B	16KB	3%	$1.6ns$

If the miss penalty to the secondary cache is 20 ns, there are 1.5 memory references per instruction (1 instruction reference and 0.5 data references) and the total instructions for the benchmark program is I.

   (a) Find the memory stall clock cycles for each machine in term of I.

   (b) Find the CPU time in term of C and I.

   (c) For what C machine B will faster than machine A?

   (d) What conclusions can you make from these calculations?

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6. (15%)

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(a) What is forwarding means in a pipelined architecture?

(b) How to do the forwarding. Using the 5-stage pipeline as example. The 5 stages are *fetch, decode (operand fetch), execute, memory reference, and write back.* During which stage is the forwarding functions?

(c) A simple program, with MIPS's instruction set architecture, is shown below:

```
loop  add  $2,  $3,  $1
      sub  $4,  $3,  $2
      add  $5,  $2,  $4
      beq  $4,  $5,  loop
      add  $8,  $5,  $2
```

Explain what the forwarding unit is doing. And if any comparisons are being made, mention them.

7. (15%)

(a) What is a *condition code* or *flag* inside a CPU?

(b) Give 4 condition codes in a typical CPU.

(c) Why condition codes are needed in a typical CPU?

(d) What are the advantages and disadvantages of using condition code?

(e) If condition code is missed in a CPU, what will happen?