

大同大學 97 學年度研究所碩士班入學考試試題

考試科目: 計算機組織

所別: 資訊工程研究所

第 1/1 頁

註: 本次考試 不可以參考自己的書籍及筆記; 不可以使用字典; 不可以使用計算器

1. (10%)
The value represented by the hexadecimal number AA BB CC DD is to be stored in an aligned 32-bit word. Assume the word address is 0008 0000₁₆
 - (a) What Endianess means? Why is it a problem?
 - (b) Show the memory content of each byte using Big Endian. Show the memory content of each byte using Little Endian.

2. (10%)
 - (a) In a typical processor, the immediate field of an instruction is restricted to 16 bit. Explain how to add a 32-bit constant, such as 0x1234ABCD to a register, i.e., R0.
 - (b) Is there is any better method to add constant 0xFFFFFFFF to register R0, assuming NOT operation is not available. Prove your answer.

3. (15%)
 - (a) What overflow means? (5%)
 - (b) In general, a processor will generate an interrupt (exception) if overflow occurs. Suppose you don't like the interrupt to occur. Show how to discover overflow within your program? You should consider two cases: signed number and unsigned number.

4. (20%)
 - (a) Show the IEEE 754 binary representation of the number -0.1₁₀ in a single precision form. Using hexadecimal form in your answer. (4%)
 - (b) What decimal number is represented by this single precision floating point number: E0 C0 00 00₁₆ ? (4%)
 - (c) What rounding bit means? What guard bit means? What sticky bit means? (8%)
 - (d) Why should we need these bits? (4%)

5. (10%)
Two different compilers are being tested for a 2.5 GHz machine with three different classes of instructions: Class A, Class B, and Class C, which require one, two, and three cycles (respectively). Both compilers are used to produce code for a large piece of software. The first compiler's code uses 5 billion Class A instructions, 2 billion Class B instructions, and 1 billion Class C instructions. The second compiler's code uses 10 billion Class A instructions, 1 billion Class B instructions, and 1 billion Class C instructions.
 - (a) Which sequence will be faster according to MIPS? (3%)
 - (b) Which sequence will be faster according to execution time? (3%)
 - (c) What is the CPI of each case? (4%)

6. (15%)
 - (a) Forwarding is a method to solve data dependence's problem. For a 5-stage pipeline, *fetch*, *decode (operand fetch)*, *execute*, *memory reference*, and *write back*, during which stage is the forwarding functions? Why? (9%)
 - (b) For each code sequence below, state whether it must stall, can avoid stalls using only forwarding, or can execute without stalling or forwarding:

Sequence 1	Sequence 2	Sequence 3
lw \$t0, 0(\$t0)	add \$t1, \$t0, \$t0	addi \$t1, \$t0, #1
add \$t1, \$t0, \$t0	addi \$t2, \$t0, #5	addi \$t2, \$t0, #2
	addi \$t4, \$t1, #5	sw \$t2, 0(\$t6)
		addi \$t3, \$t2, #4
		addi \$t5, \$t0, #6

7. (20%)
 - (a) Why a modern processor needs cache? (4%)
 - (b) Why cache works for modern processor? (4%)
 - (c) Explain the possible organizations of a cache system? (4%)
 - (d) A computer system has L1 and L2 caches. The local hit rates of L1 and L2 are 95% and 80%, respectively. The miss penalties are 8 and 60 cycles. Assuming a CPI of 1.2 without any cache miss and average of 1.1 memory access per instruction, what is the effective CPI after cache misses are factored in?