大同工學院 87 學年度研究所招生入學考試試題

考試科目 計算機組織　　所別 通訊工程研究所

註：本次考試 [不可] 參考自己的書籍及筆記 [不可] 查字典 [可] 使用計算器

(20%) 1. Suppose that two unsigned binary integers $X = x_0x_1x_2$ and $Y = y_0y_1y_2$ are to be multiplied.

(a) Design a 3-bit combinational multiplier with two-bit AND gates and full adders.

(b) Design a 3-bit combinational multiplier using the cell *M*. Suppose that *M*'s output *y* and *z* are the carry-out and sum of the arithmetic expression of $ac+b+d$ where *a*, *b*, $\bar{c}$, and $\bar{d}$ are *M's* inputs..

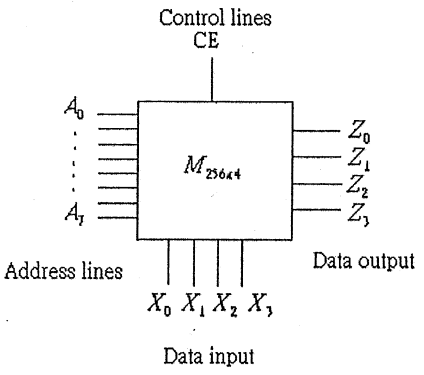
(10%) 2. Compare peripheral processors and coprocessors in the hardware implementation of floating-point instructions, considering programming requirements, processing speed, and communication with the host CPU.

(20%) 3. Encode the microinstructions described below so that the minimum number of control bits is used and all inherent parallelism among the microoperations is preserved.

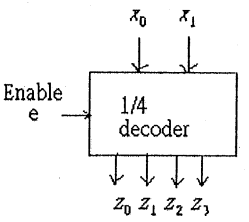
Table 1

Microinstruction	Control signals activated
I_1	*a, b, c, g*
I_2	*a, c, e, h*
I_3	*a, d, f*
I_4	*b, c, f*

(15%) 4. A 2K x 8-bit RAM is to be designed from 256 x 4-bit RAM ICs. Assume that 1-out-of-4 decoder ICs are also available, as well as ICs containing standard logic gates. The main design goal is to minimize the total number of ICs used. Carry out the design assuming that each RAM chip has a single chip-enable line CE. Give your answer by using the following block diagrams of 256 x 4-bit RAM and 1-out-of-4 decoder in Figure 1.



(a) 256 x 4-bit RAM ICs



(b) 1/4 decoder

Figure 1

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(10%)5. Consider a two-level memory hierarchy of the form (M_1, M_2) where M_1 is connected directly to the CPU. Let c_i and S_i denote the cost per bit and total storage capacity of M_i for $i = 1,2$. Let t_{A_i} be the access time of M_i, i.e., the average time to read one word from M_i to its own output port. Define the *hit ratio* H_i associated with the memory M_i at level i as the probability that the information requested by the CPU has been assigned to M_i. Determine the average cost per bit c and the average access time t_A (with respect to the CPU) for the data given in Table 2.

Table2

Level i	Capacity S_i	Cost c_i(\$/bit)	Access time t_{A_i}(s)	Hit ratio H_i
M_1(main)	2^{16}	0.001	10^{-7}	0.9
M_2(secondary)	2^{24}	0.00001	10^{-4}	1.0

(10%) 6.What are the differences between the following contrasting pairs of terms in the context of computer networks: (a) Twisted pair vs coaxial cable (b) Simplex vs duplex (c) Circuit switching vs packet switching (d) Local area vs wide area (e) Baseband vs broadband.

(15%) 7. (a) List the advantages and disadvantages of designing a floating-point processor in the form of k-segment pipeline rather than a k-unit parallel processor. (b) A floating-point pipeline has four segments S_1, S_2, S_3, and S_4 whose delays are 100, 90, 100, and 110 ns, respectively. What is the pipeline's maximum throughput in MFLOPS? Explain the reasons for the answer.

Starvation.